

ENABLING AI Infrastructure

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Agenda

- ① **Enabling AI Infrastructure:** Charlie Kawwas
- ② **Scalable AI Networks:** Ram Velaga
- ③ **AI Server Interconnect:** Jas Tremblay
- ④ **Optical Interconnects:** Near Margalit
- ⑤ **Foundational Technology for AI Interconnect:** Vijay Janapaty
- ⑥ **Custom AI Accelerators:** Frank Ostoic
- ⑦ **Closing Remarks:** Charlie Kawwas

ENABLING AI Infrastructure

Charlie Kawwas, Ph. D.
President, Broadcom

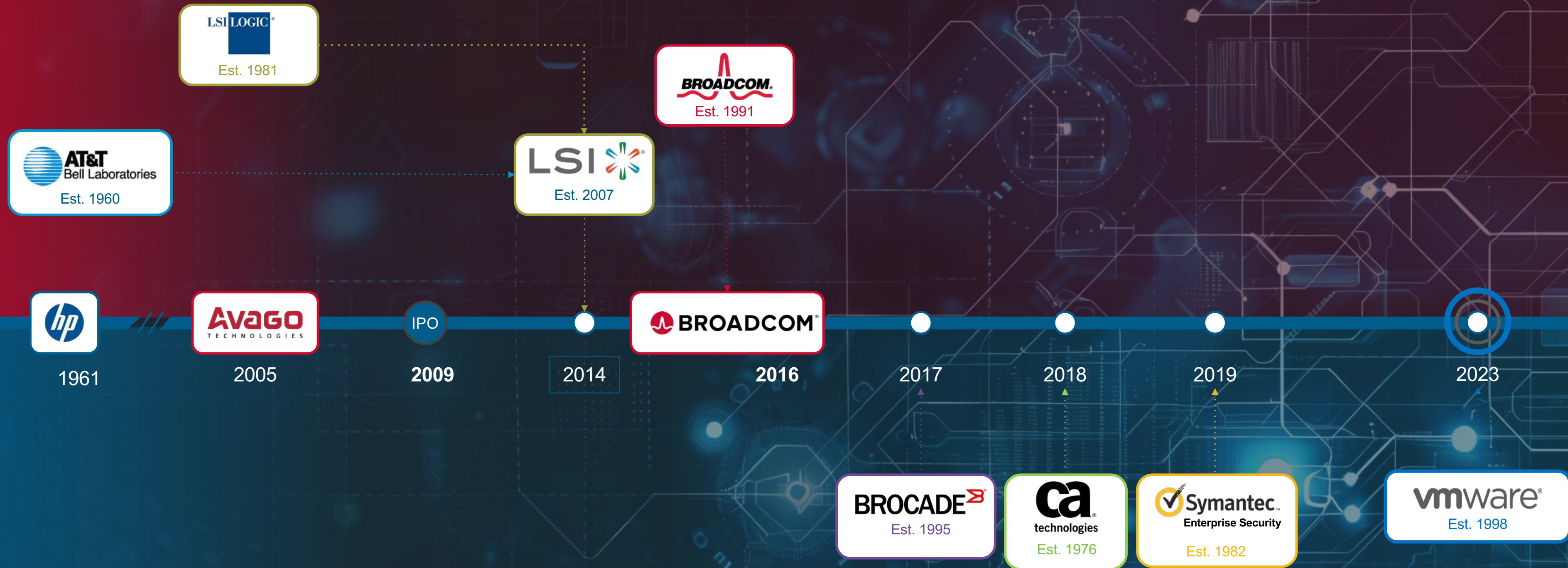


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Heritage of Technology Innovation

Semiconductors

Infrastructure Software



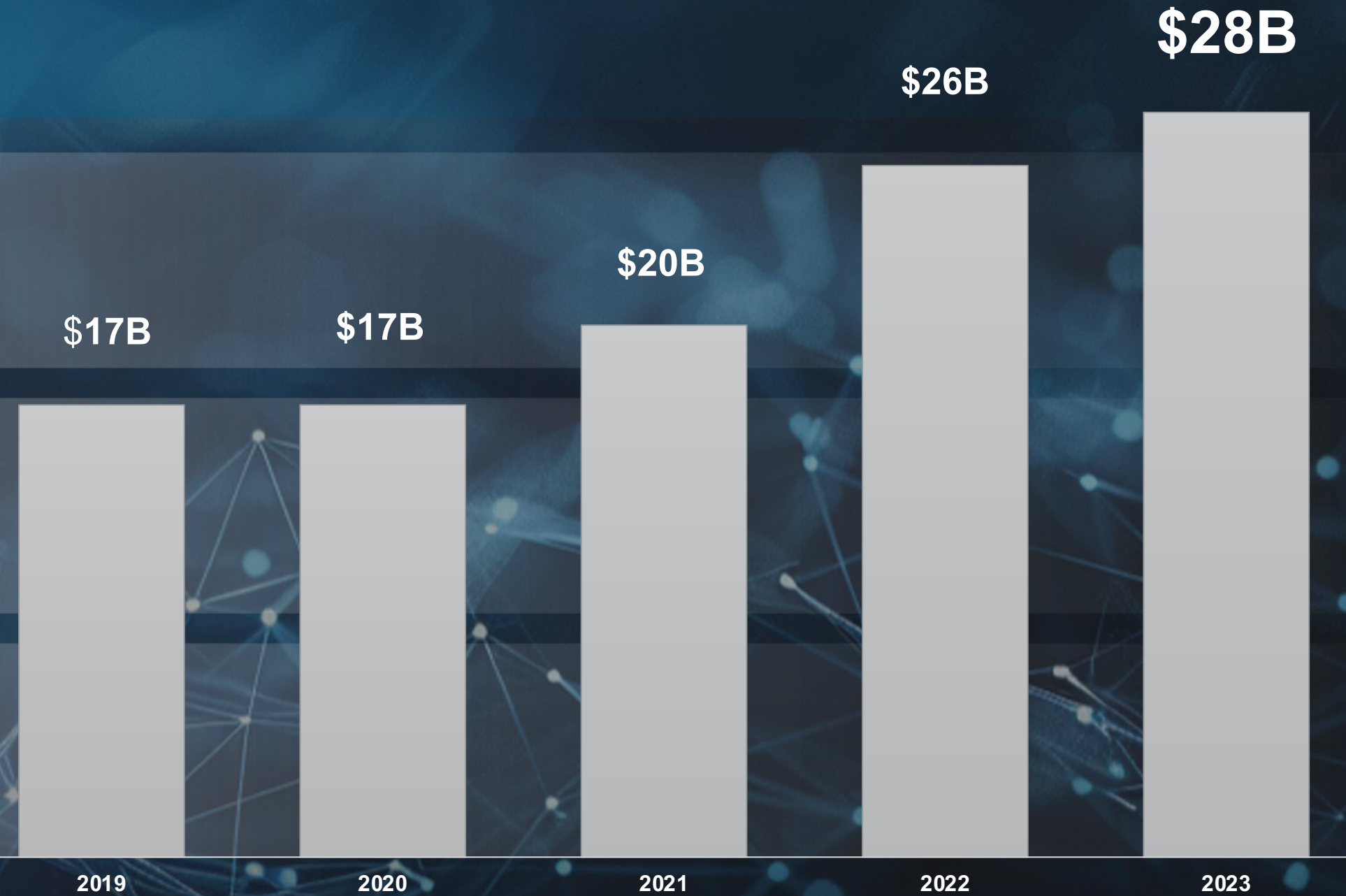
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Semiconductors

FY23 Revenue **\$28B**

2019-2023 CAGR **13%**

Annual R&D spend **\$3B+**



Technology Leadership → Organic Growth

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Strategy

Market

10 Year Horizon

Technology

Leadership

Execution

Excellence

**Sustainable
Franchise**

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Strategy

Market

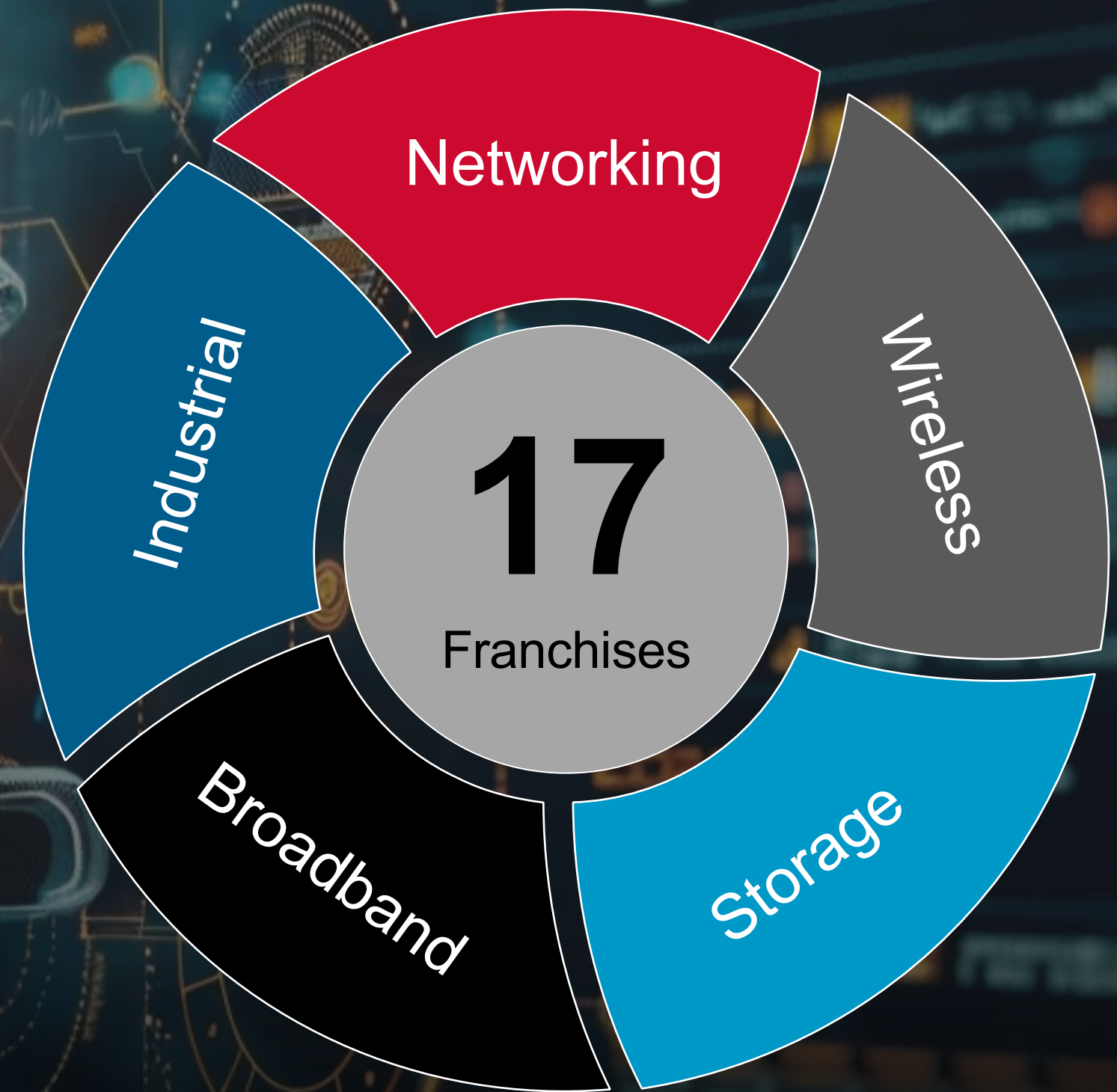
10 Year Horizon

Technology

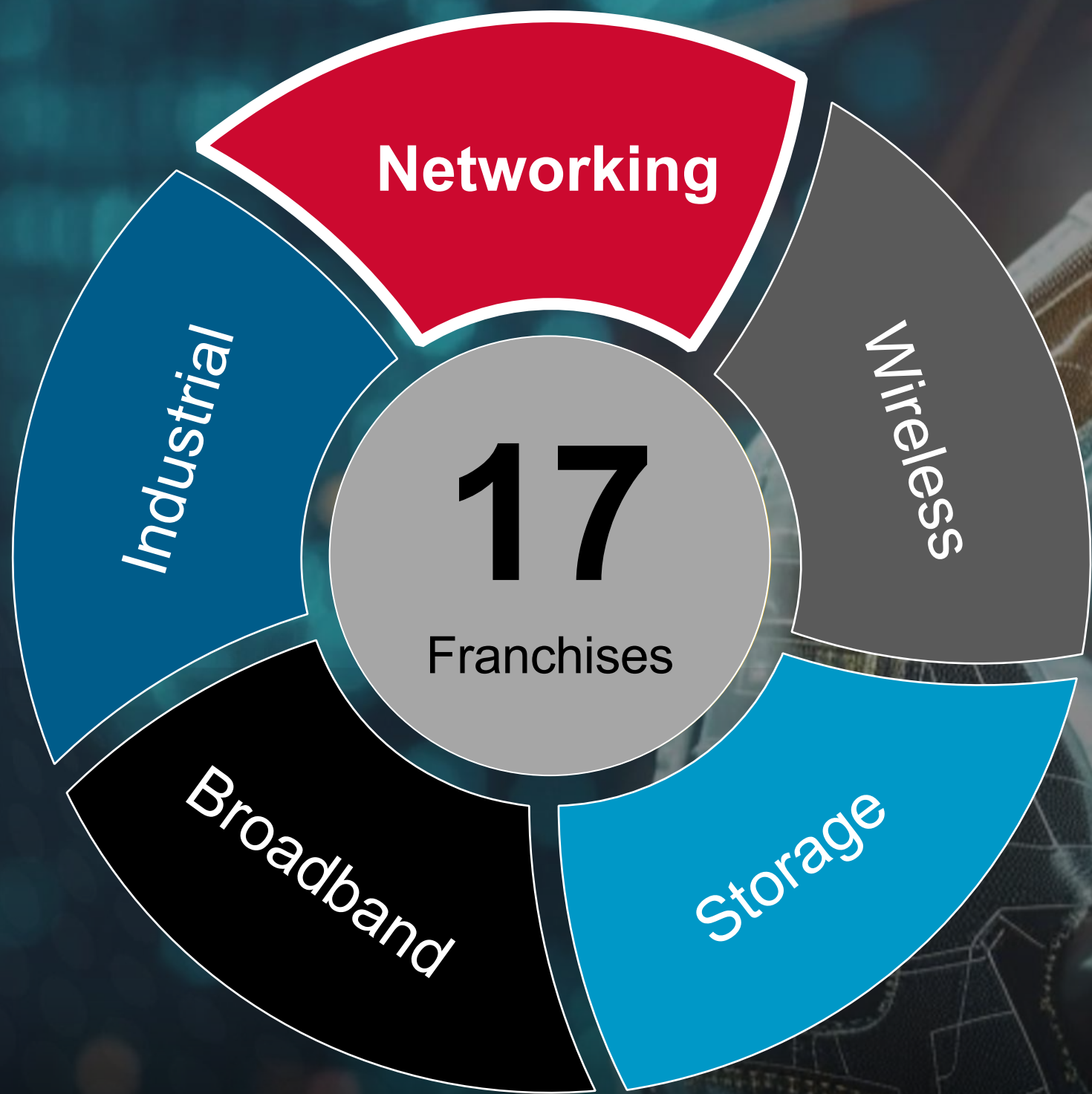
Leadership

Execution

Excellence

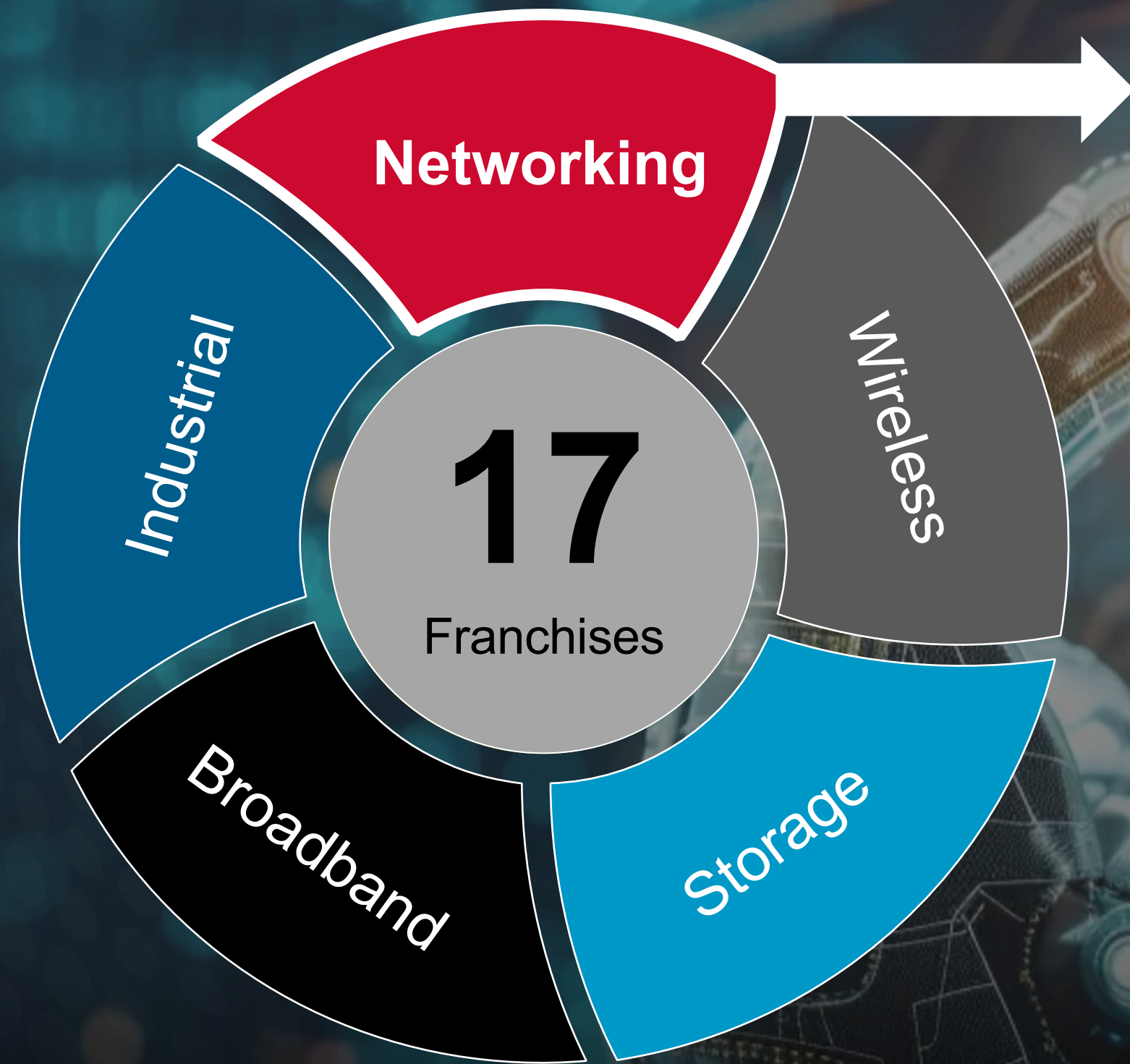


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Enabling AI infrastructure



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Two AI Markets

Consumer AI

Search, Social Networking, ...

Enterprise AI

Public Cloud, On-Prem, ...

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Consumer AI

Search, Social Networking, ...

Enterprise AI

Public Cloud, On-Prem, ...

AI Accelerators (XPU)

Custom

Merchant

AI Connectivity

Merchant

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Consumer AI

Search, Social Networking, ...

Enterprise AI

Public Cloud, On-Prem, ...

AI Accelerators (XPU)

Custom

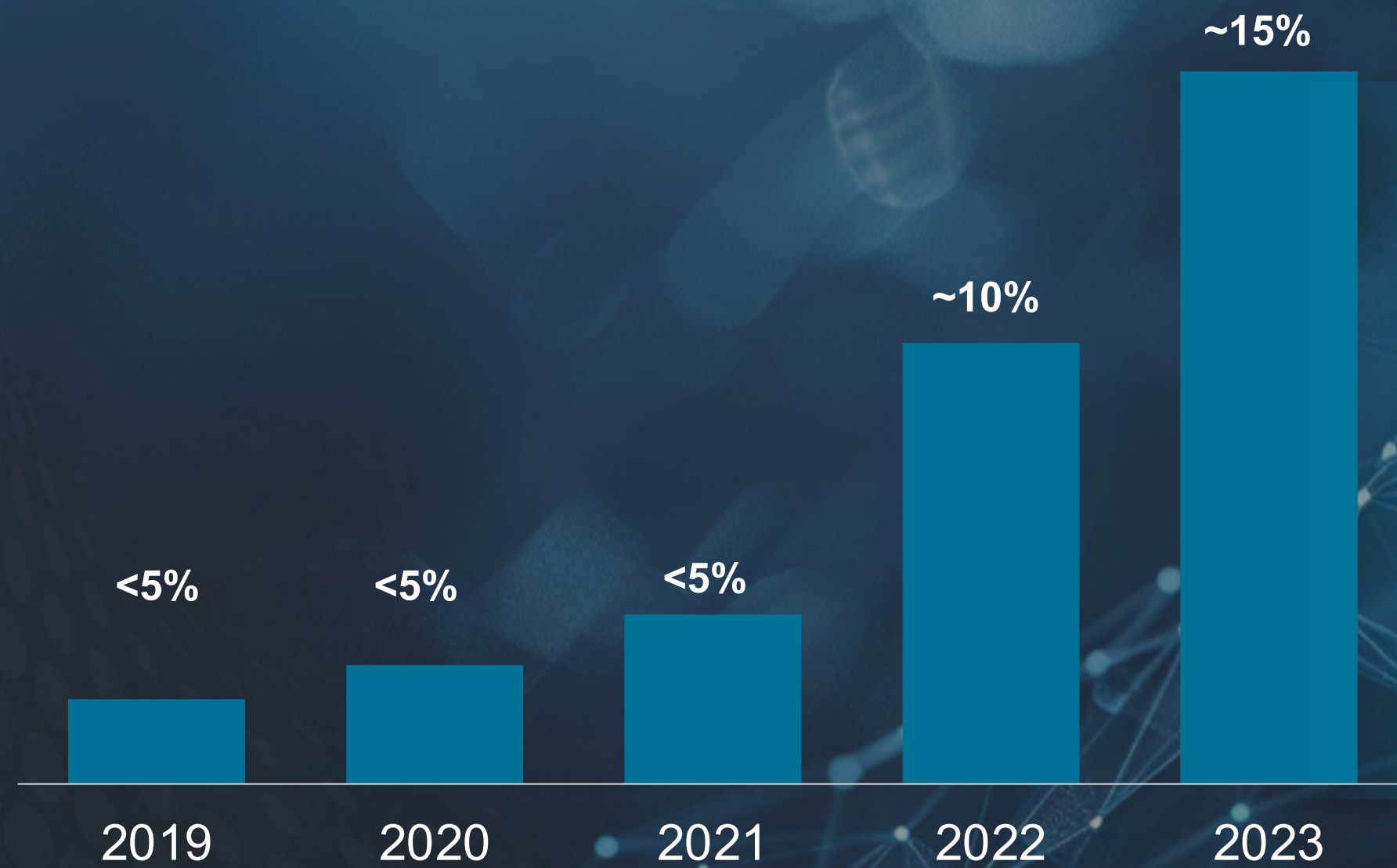
Merchant

AI Connectivity

Merchant

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Broadcom's AI Journey...

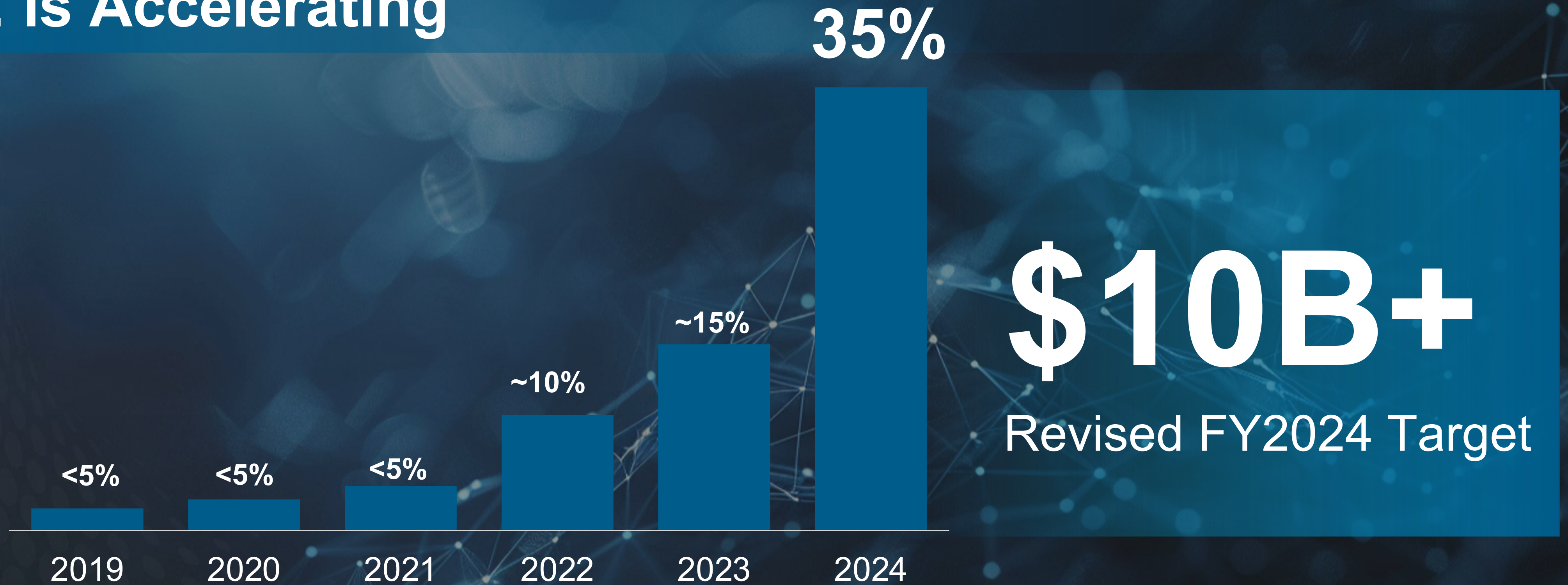


AI Revenue as % of Semiconductor Solutions Revenue

25%
FY2024 Target

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... is Accelerating



AI Revenue as % of Semiconductor Solutions Revenue

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XPUs → Multi-Generational strategic engagements

2024

2025

2026

Customer #1

Production



Customer #2

Production



Customer #3

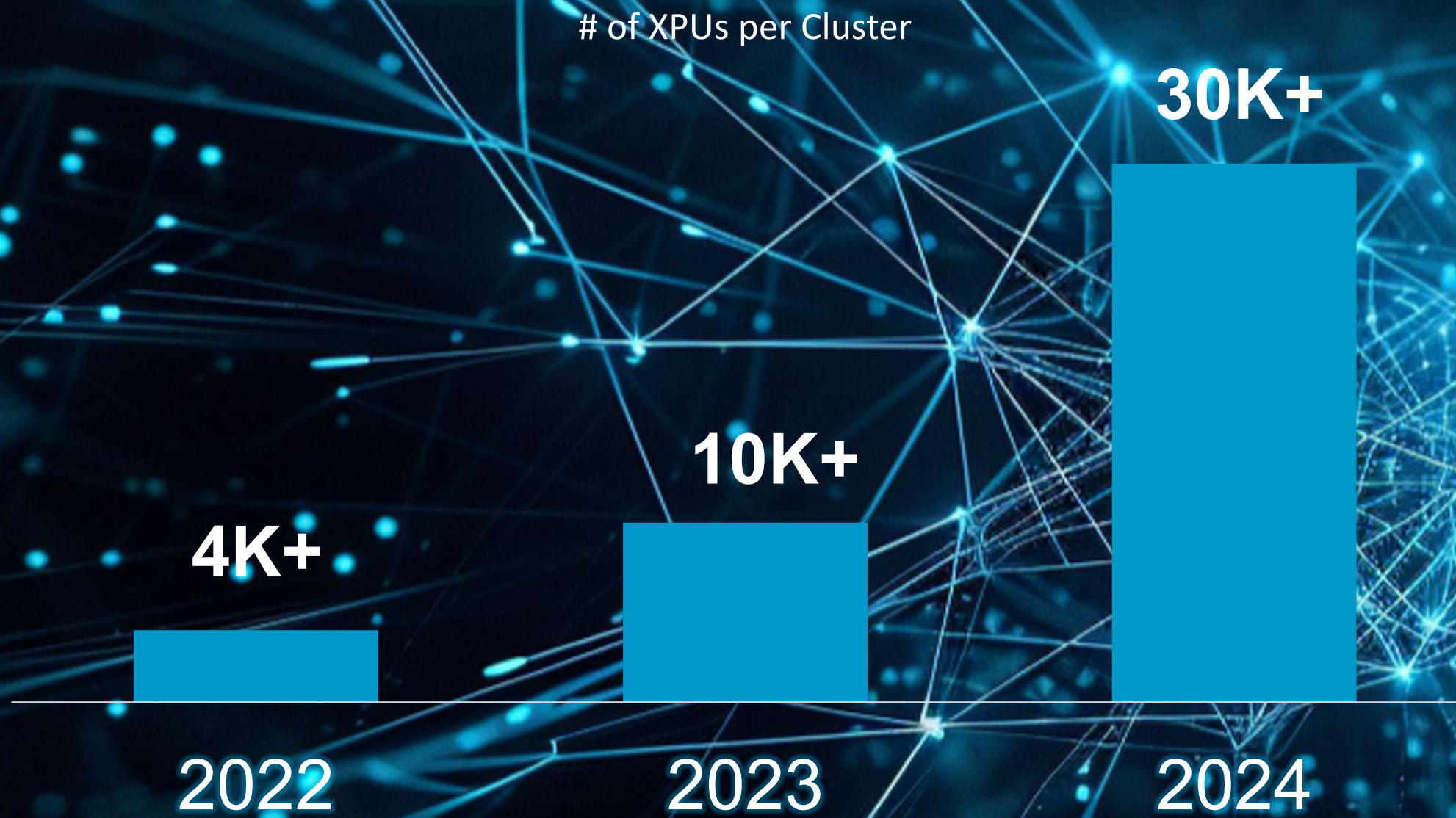
New

Ramp →
Production



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The Build-Out is On...



1M?

2027+

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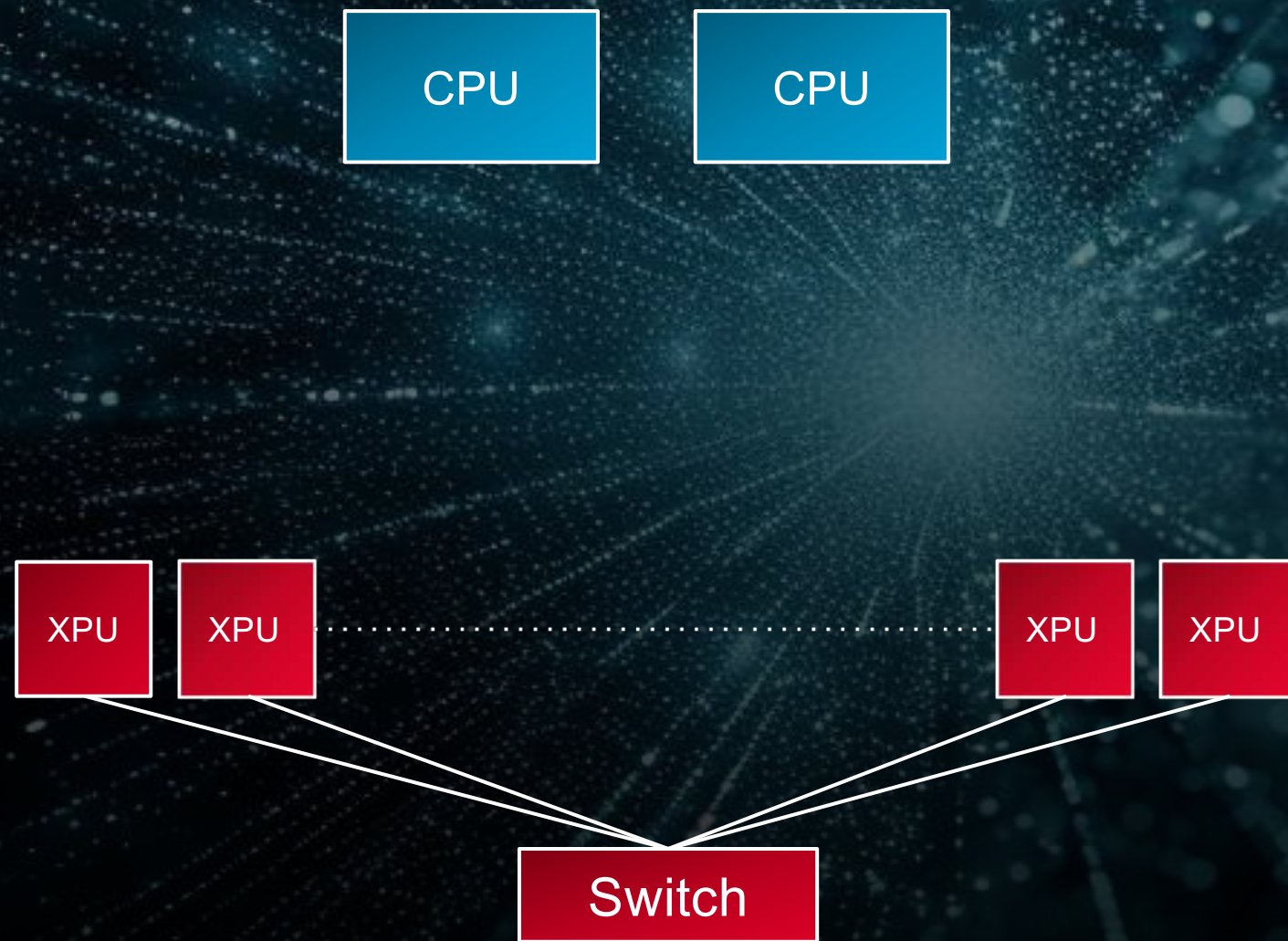
XPU

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Scale Up



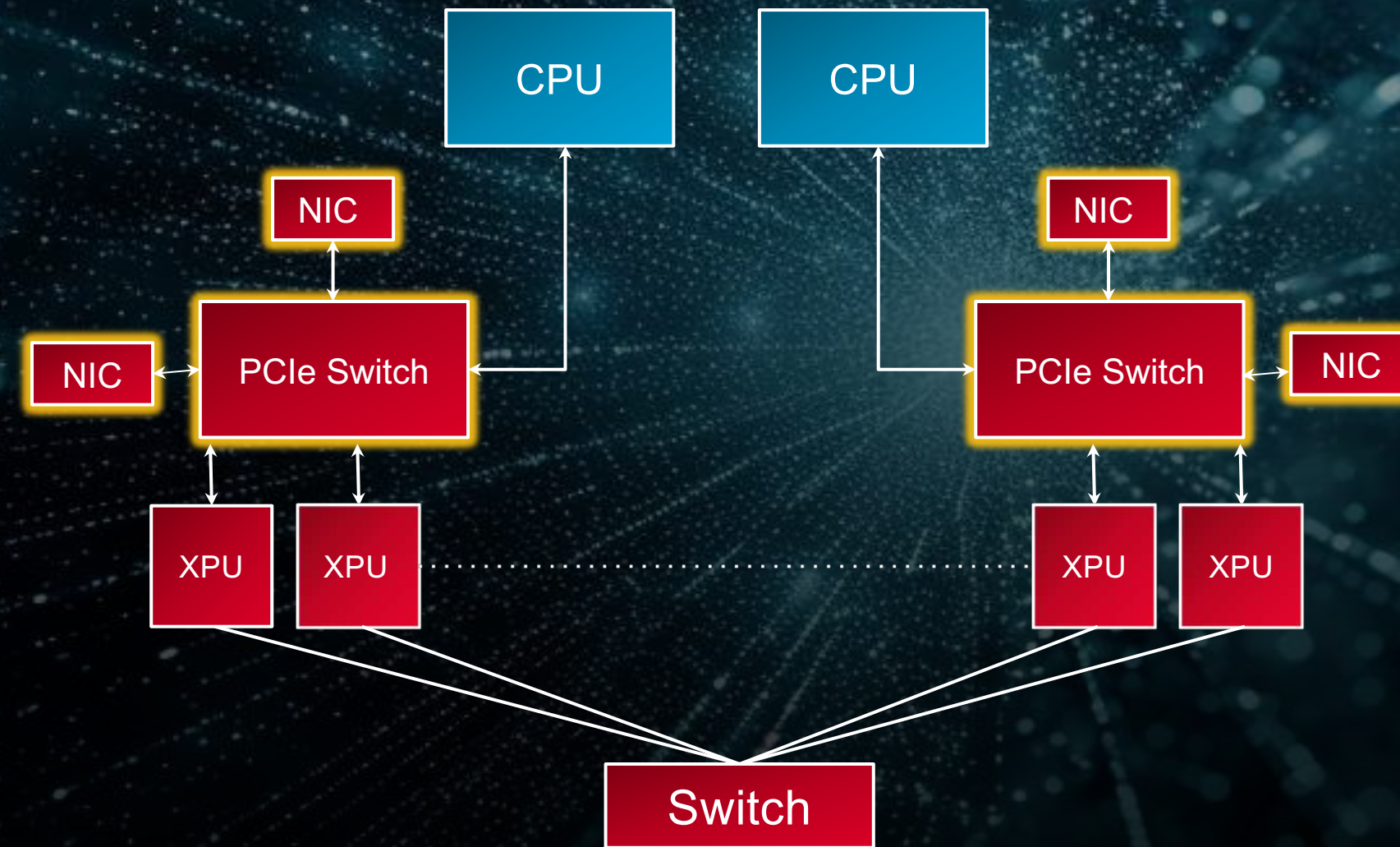
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Scale Up

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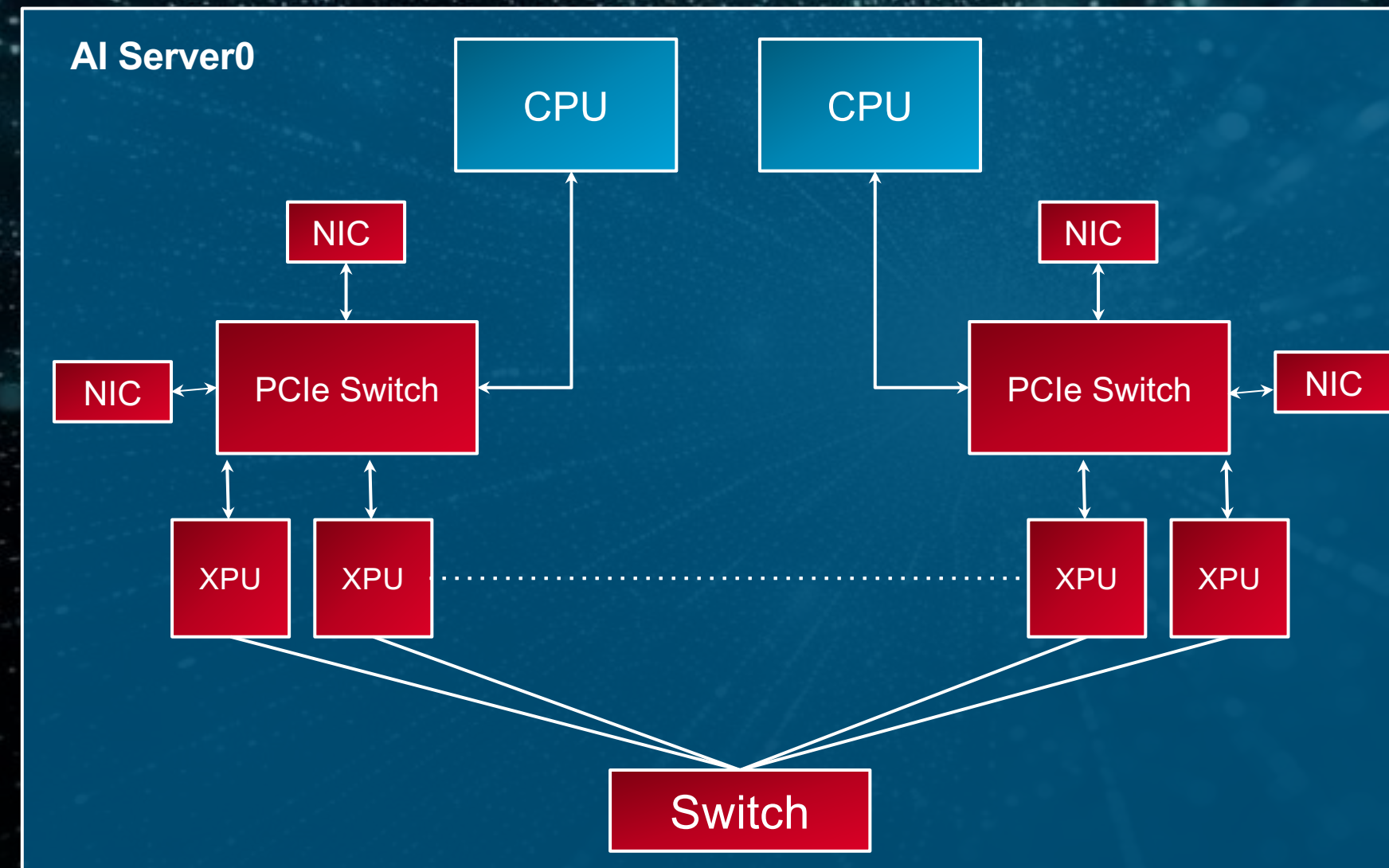
Interconnect



Scale Up

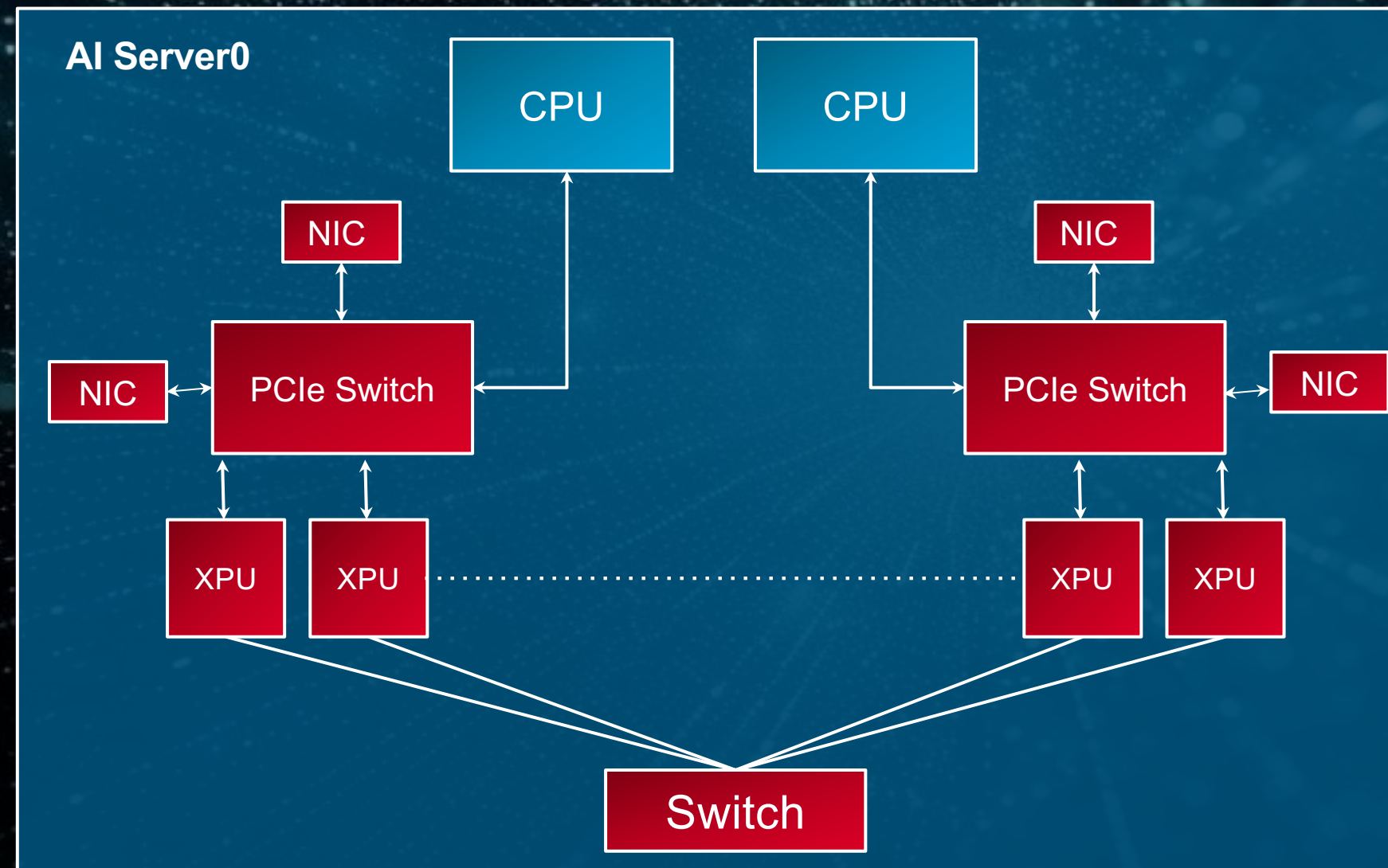
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Interconnect



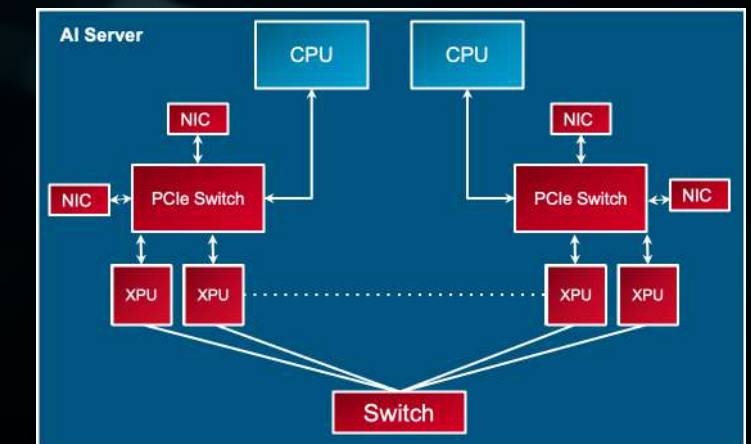
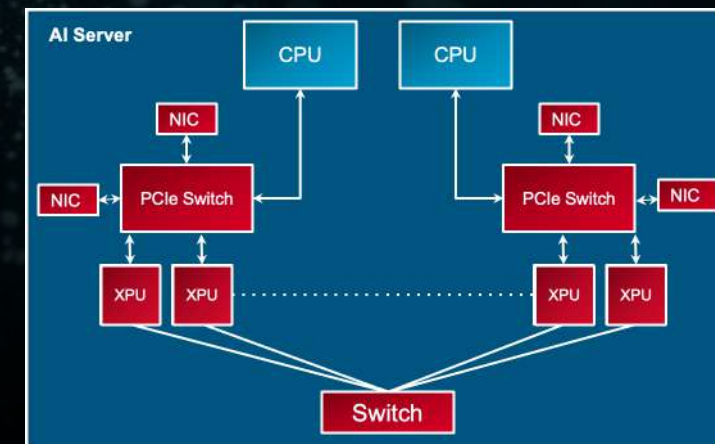
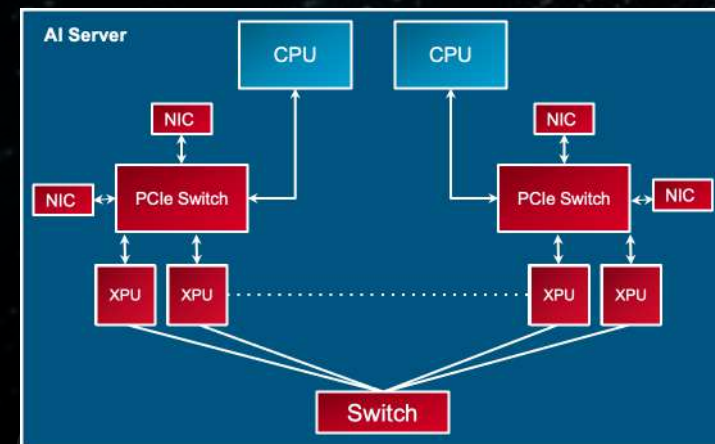
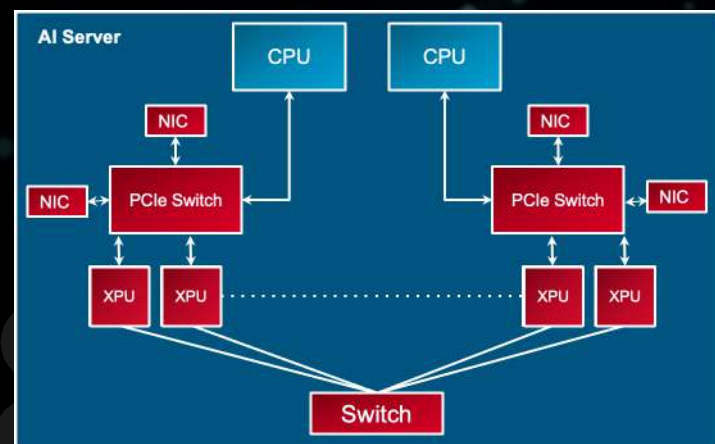
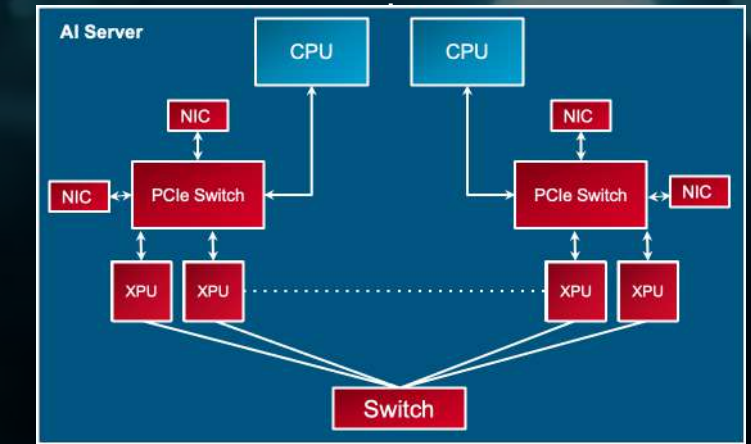
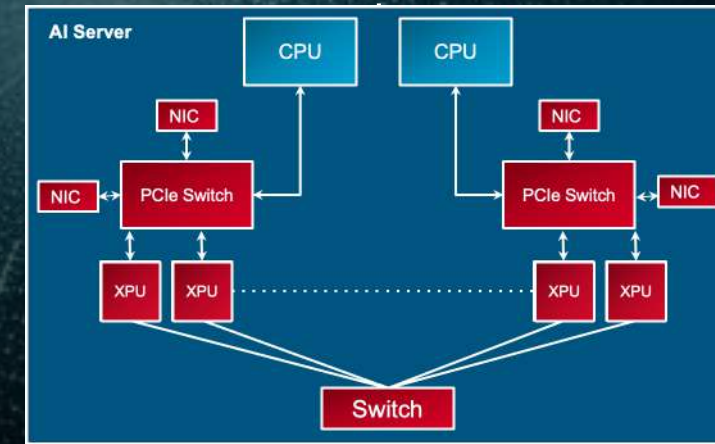
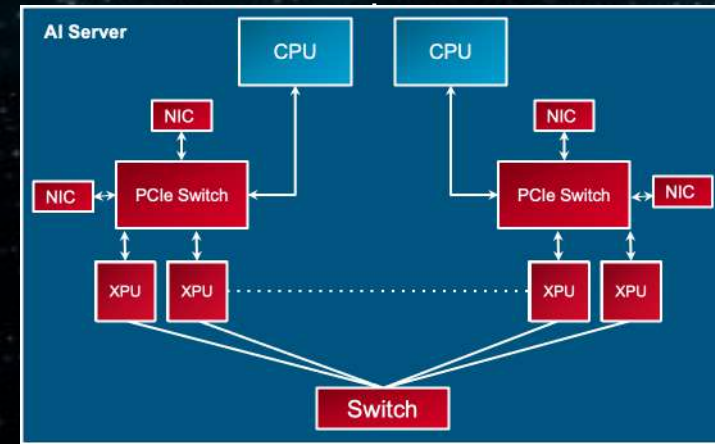
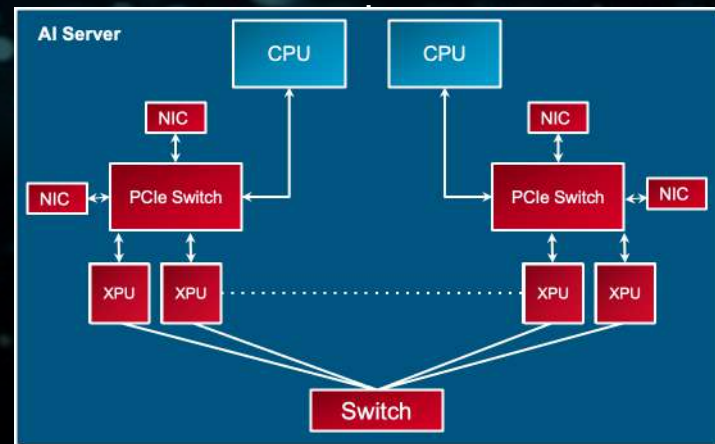
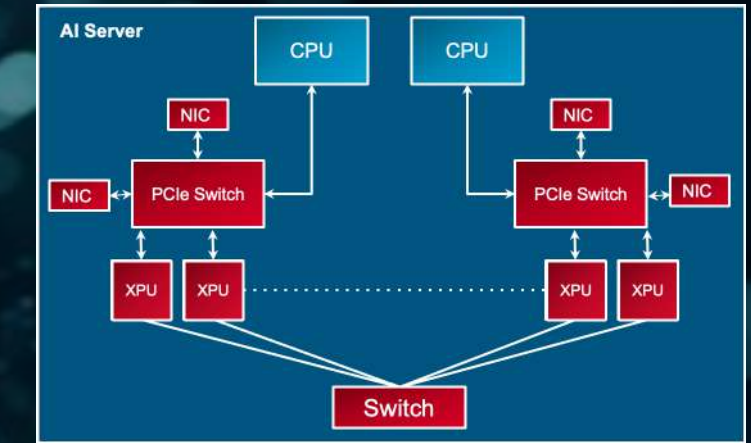
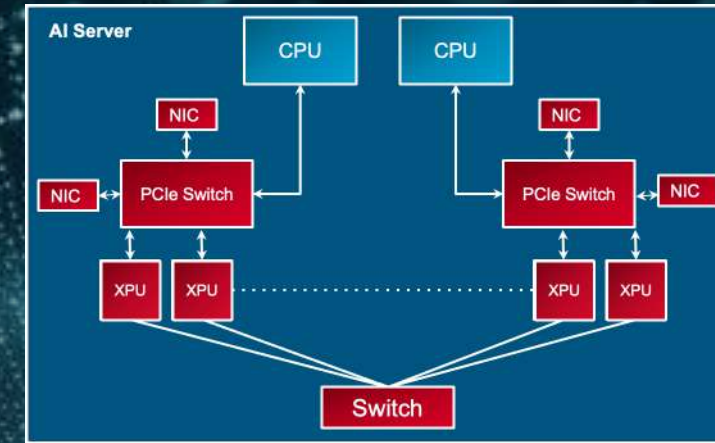
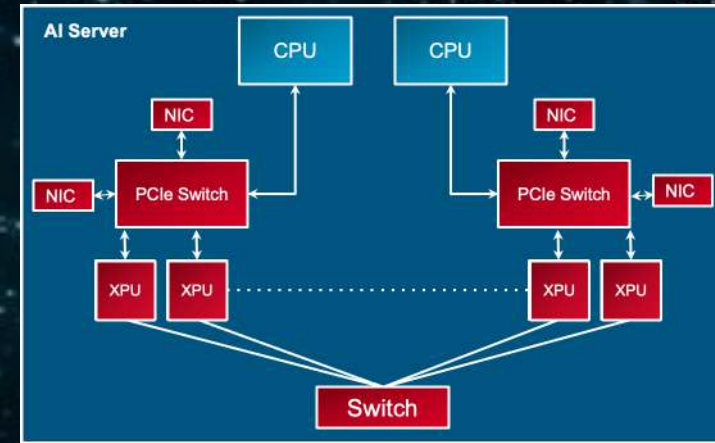
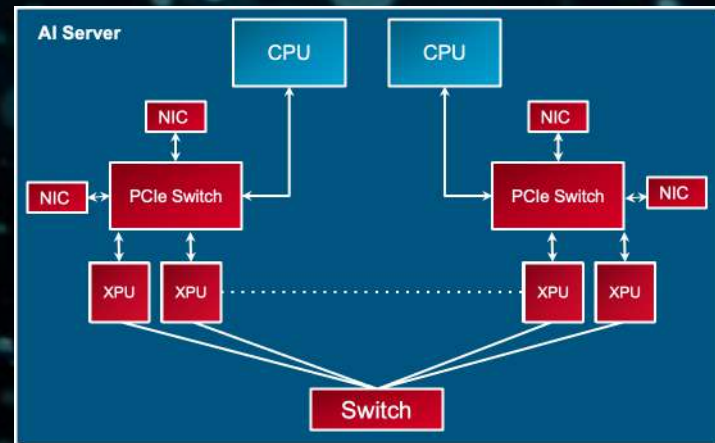
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→ Broadcom SAM



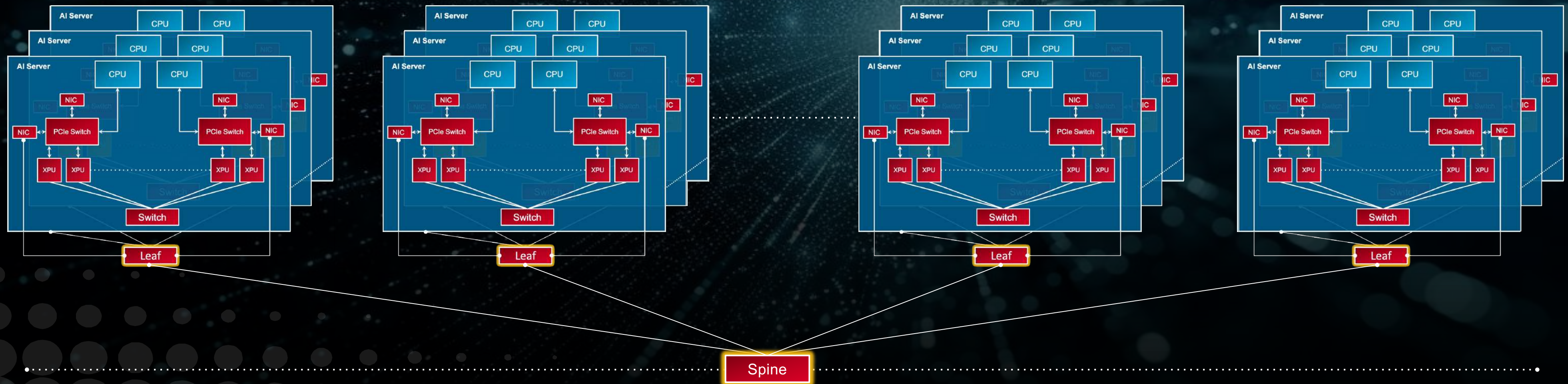
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Scale Out



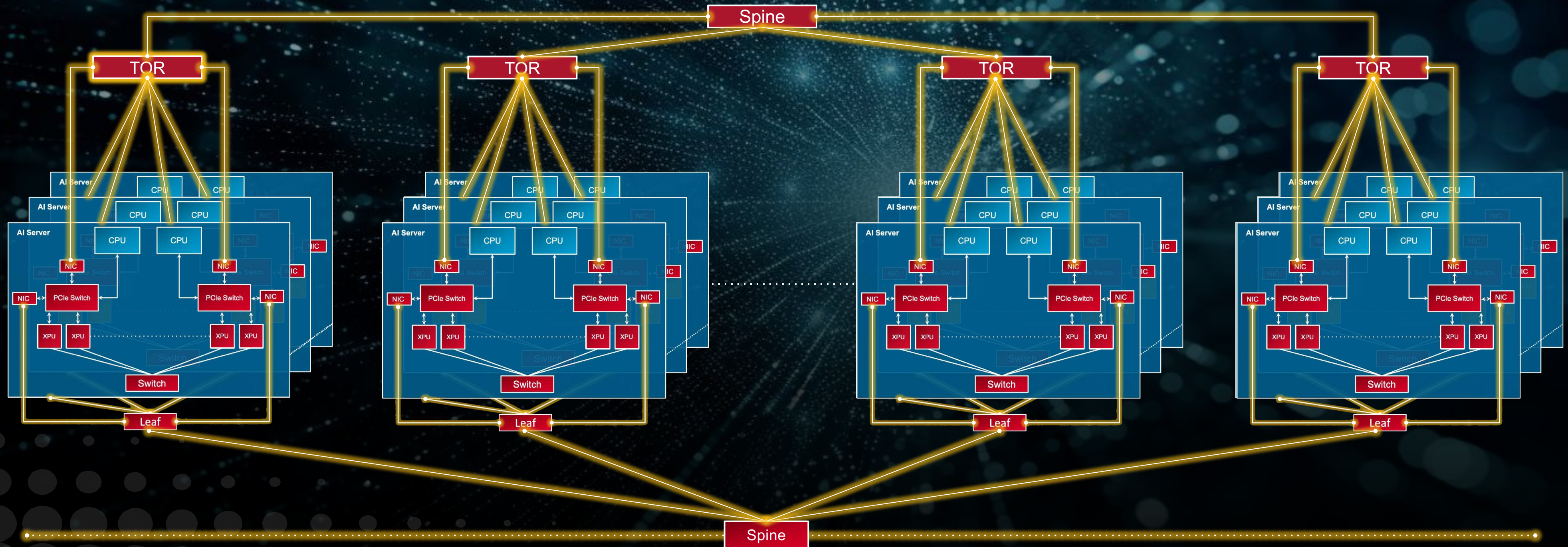
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Scale Up + Scale Out = Back End



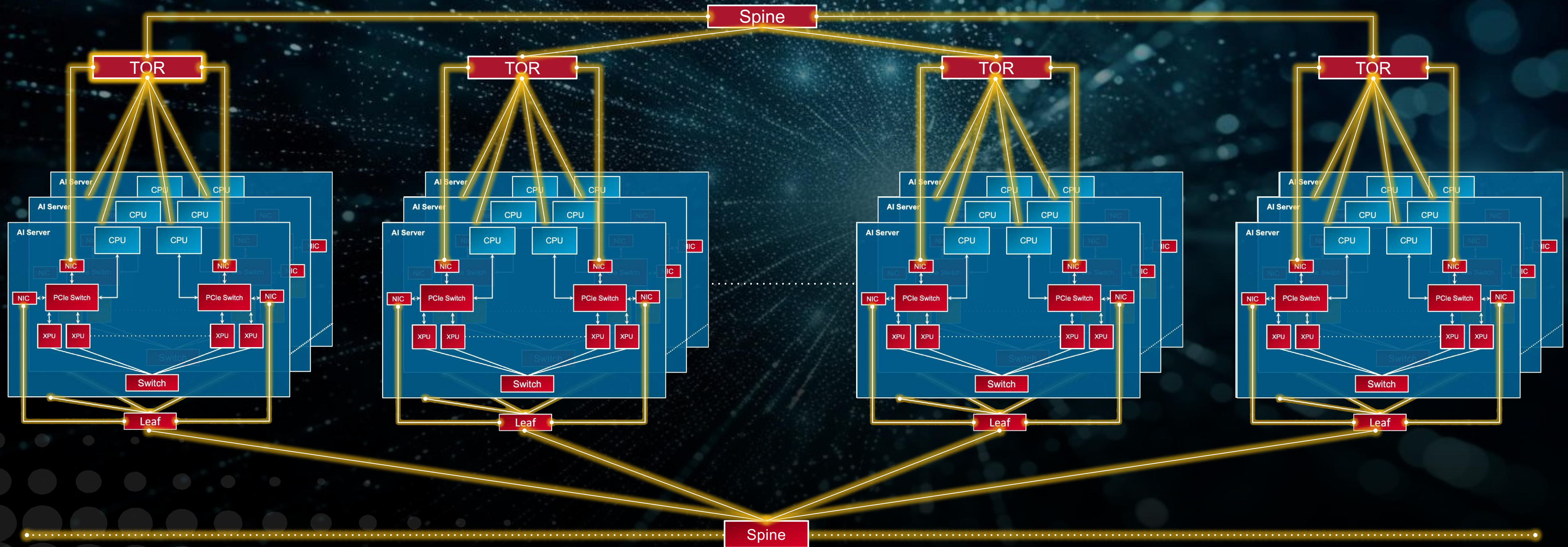
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Interconnect



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→ Broadcom SAM

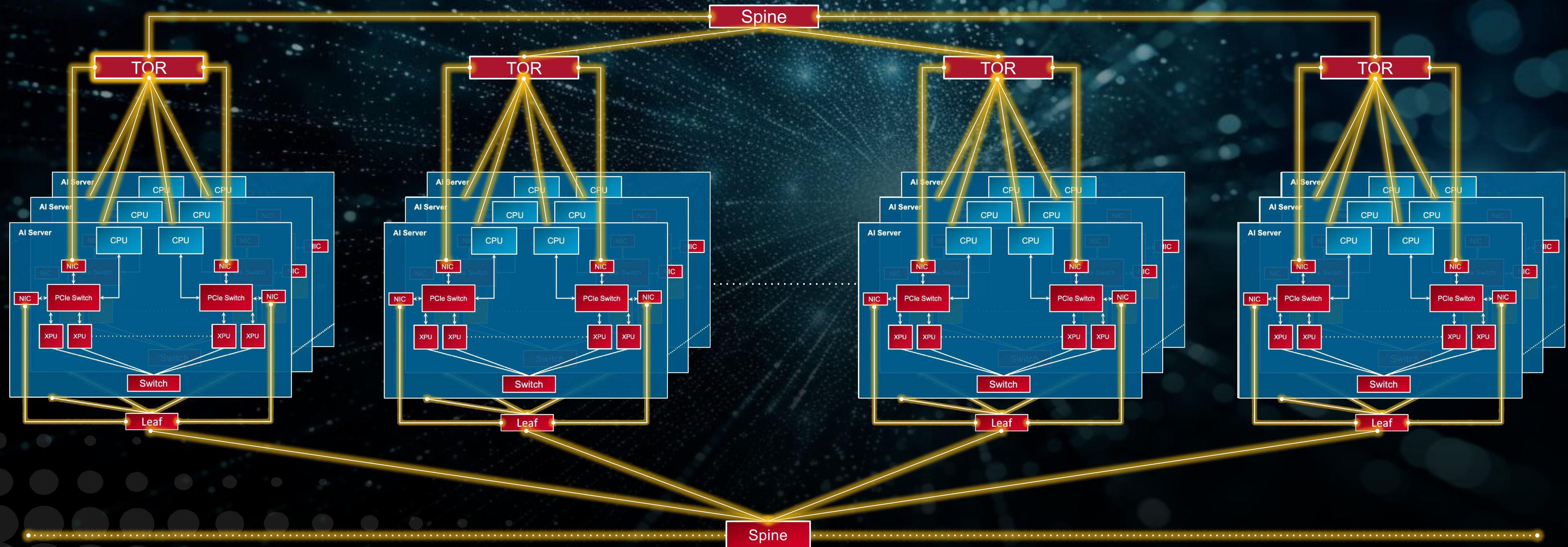


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1. Power

2. Complexity

3. Ecosystem



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Open Scalable Power Efficient

Sustainable Technology Leadership

Ethernet

PCIe

Optics

SerDes

DSP

Custom

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Scalable AI Networks

Ram Velaga

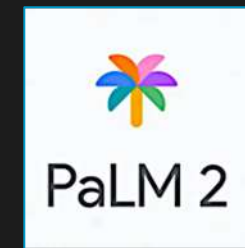
General Manager
Core Switching Group
Broadcom



New AI Models → 100X+ Scale → Distributed Computing

1 Million

AI Accelerators



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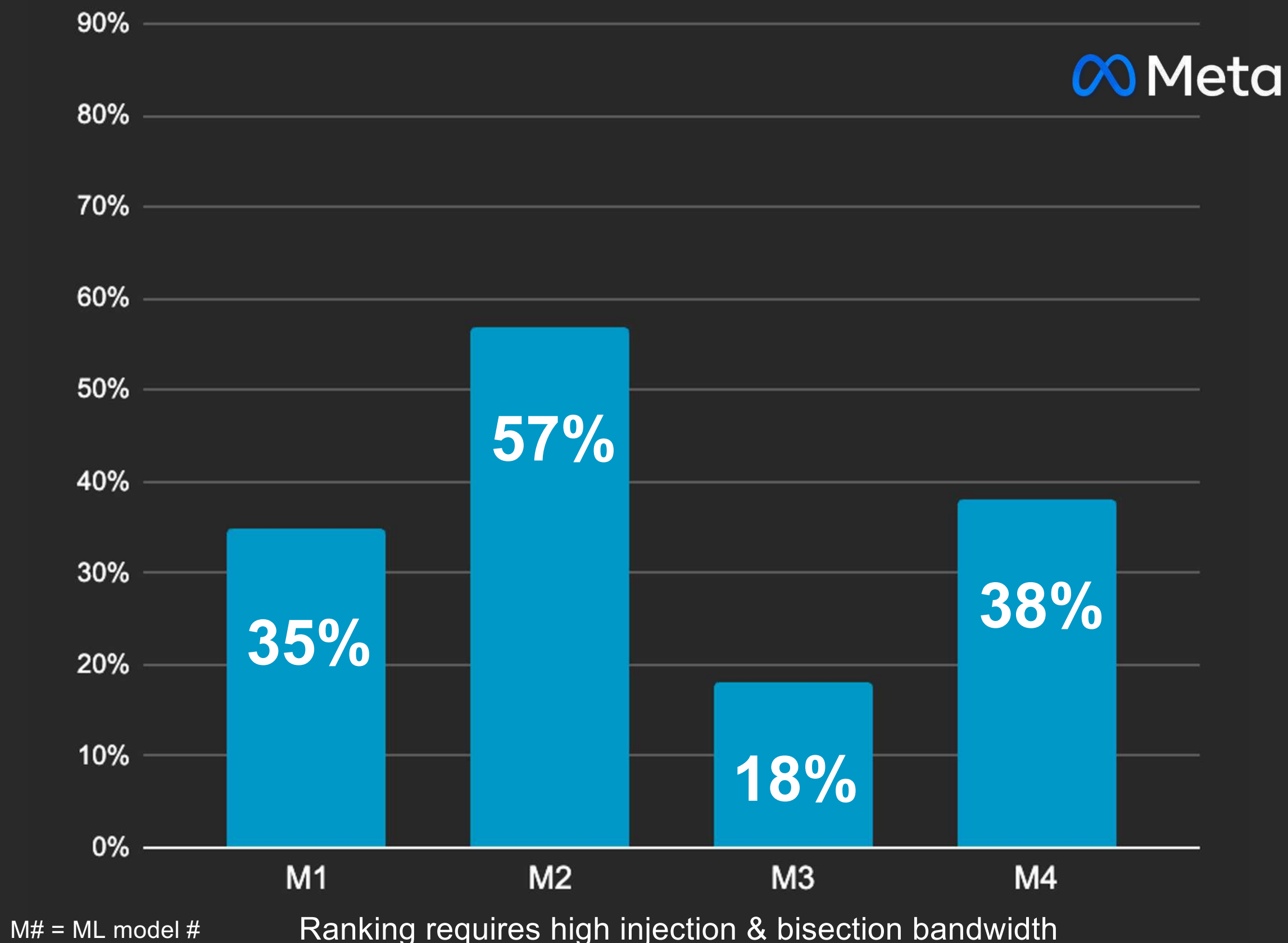
THE NETWORK IS THE COMPUTER

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“ Network I/O is Key for Recommendation Workloads. ”

Meta, OCP 2022 Global Summit

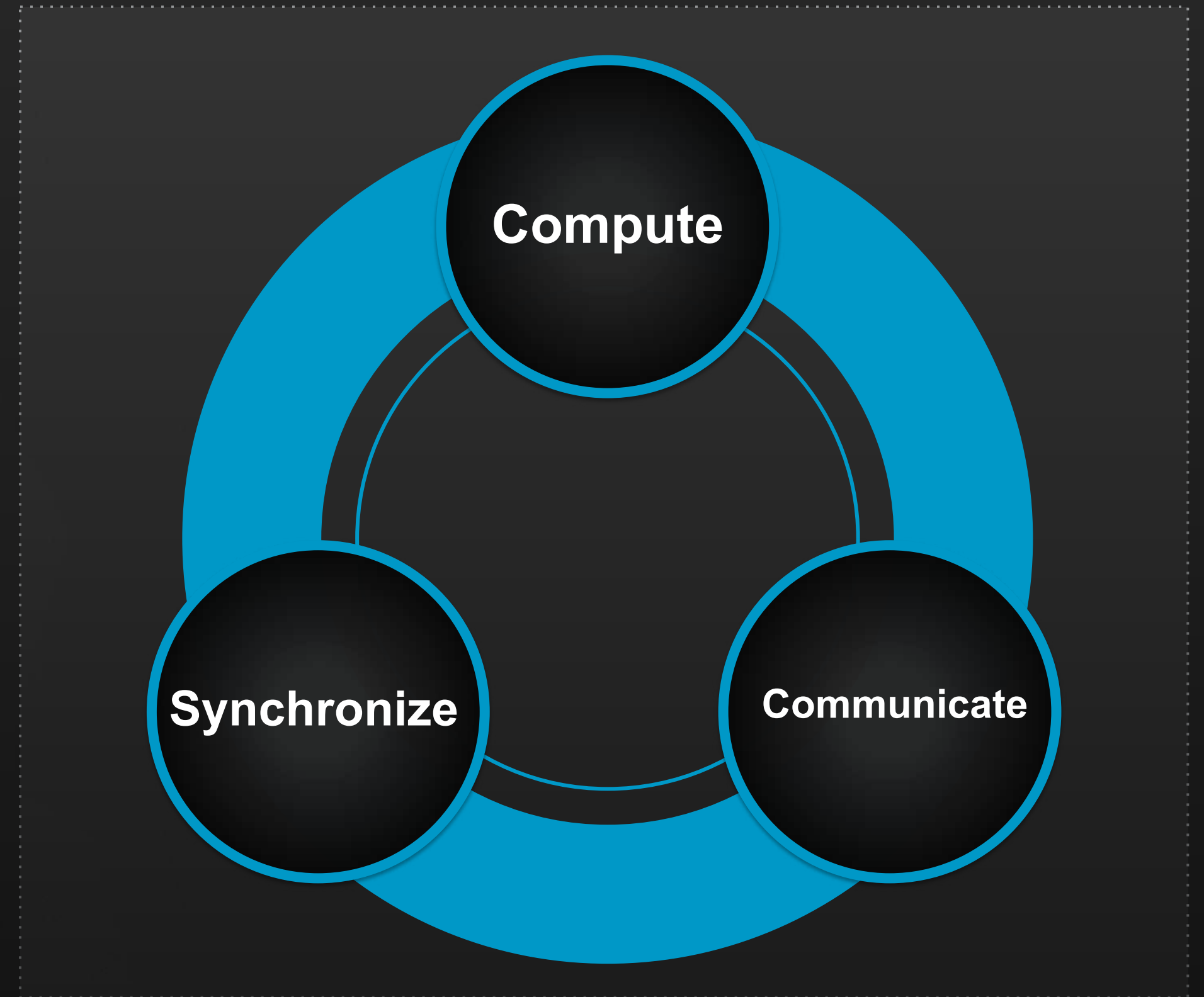
TIME SPENT IN NETWORKING



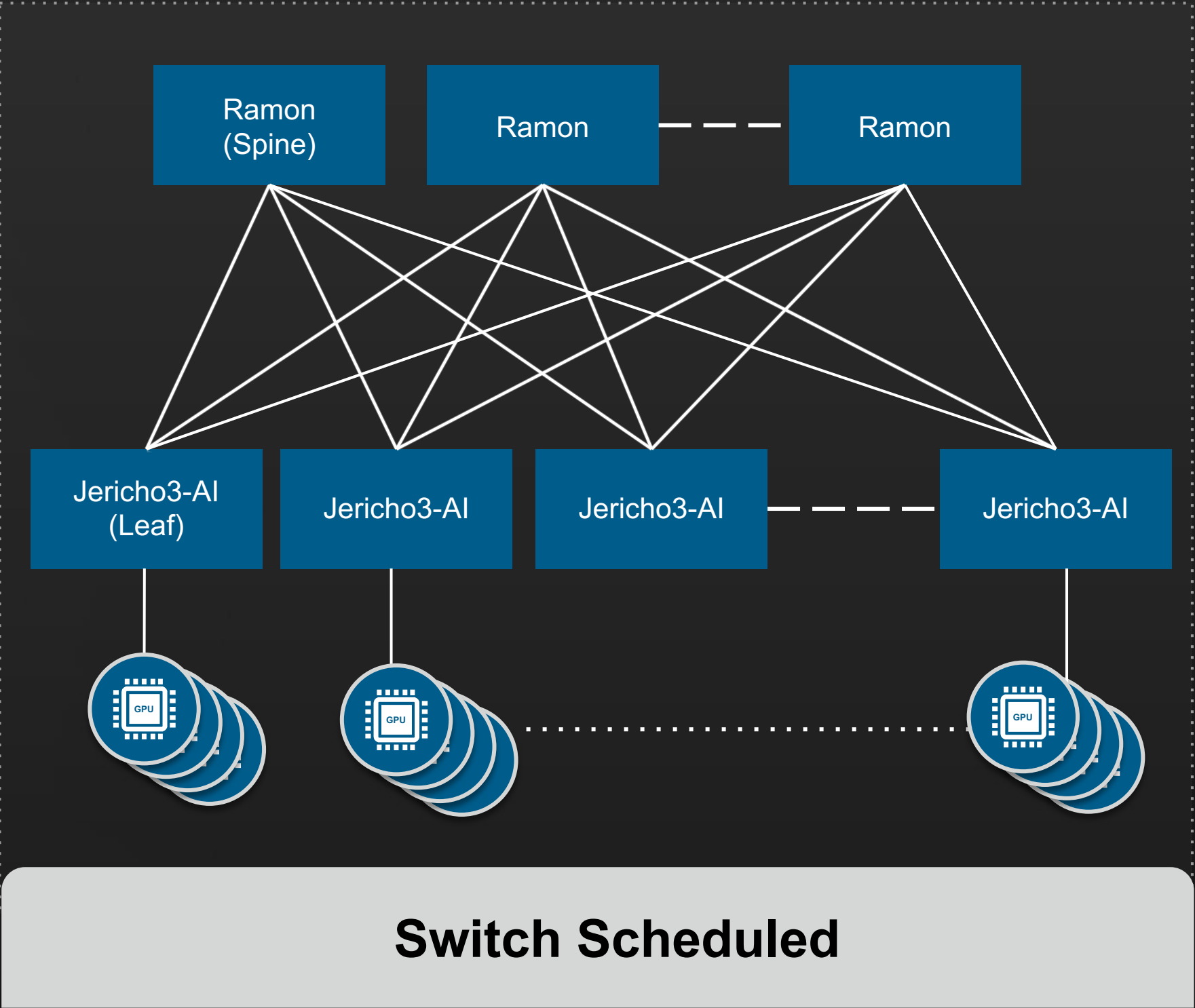
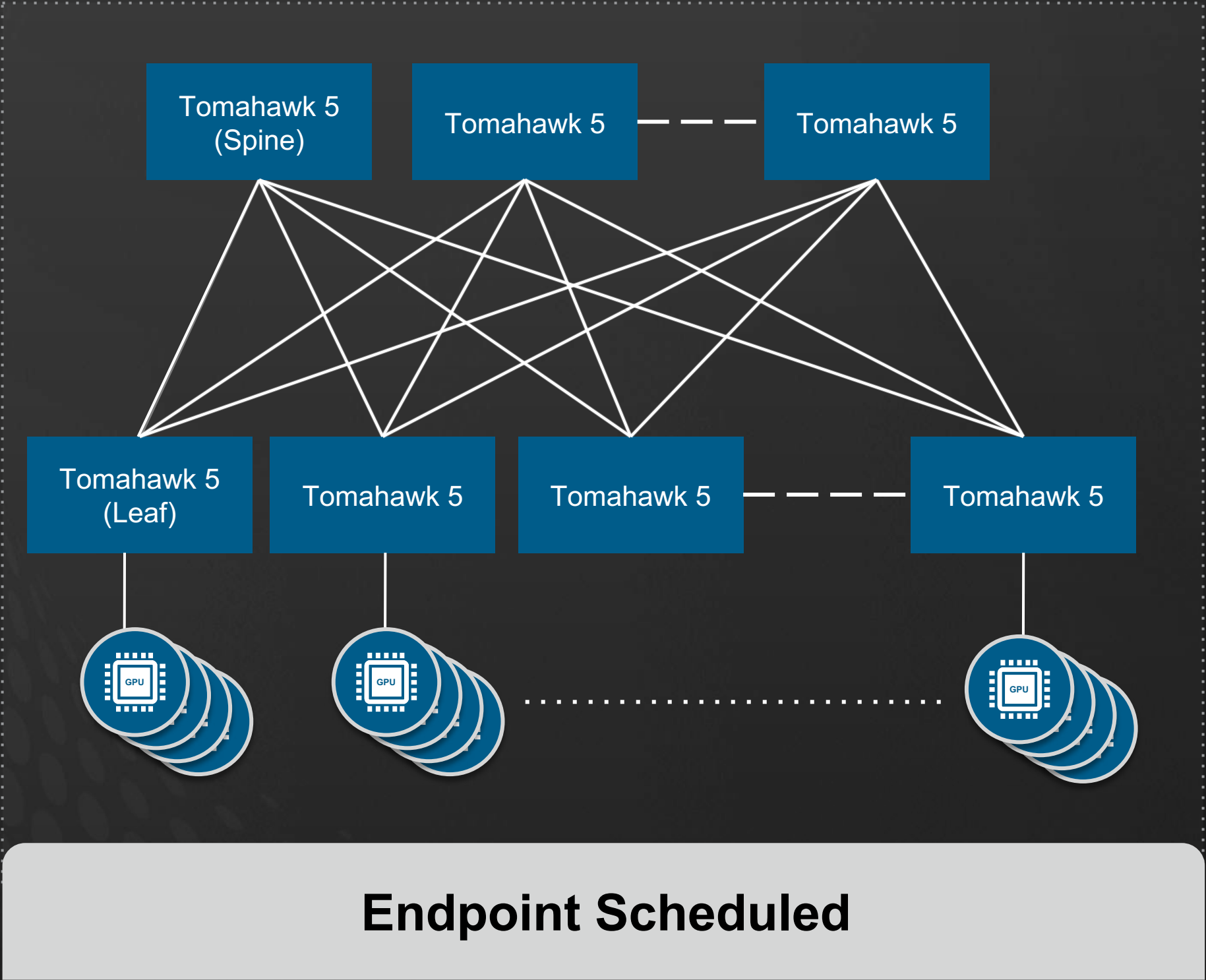
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What Makes AI Networks Unique?

- Very high bandwidth
- RDMA traffic → Bulk data transfers
- Intermittent data surges
- Straggler data significantly impacts job completion time
- Training jobs run over long durations (hours, days)



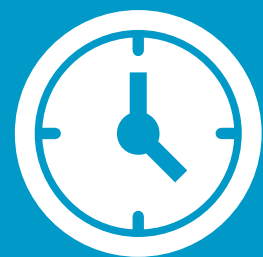
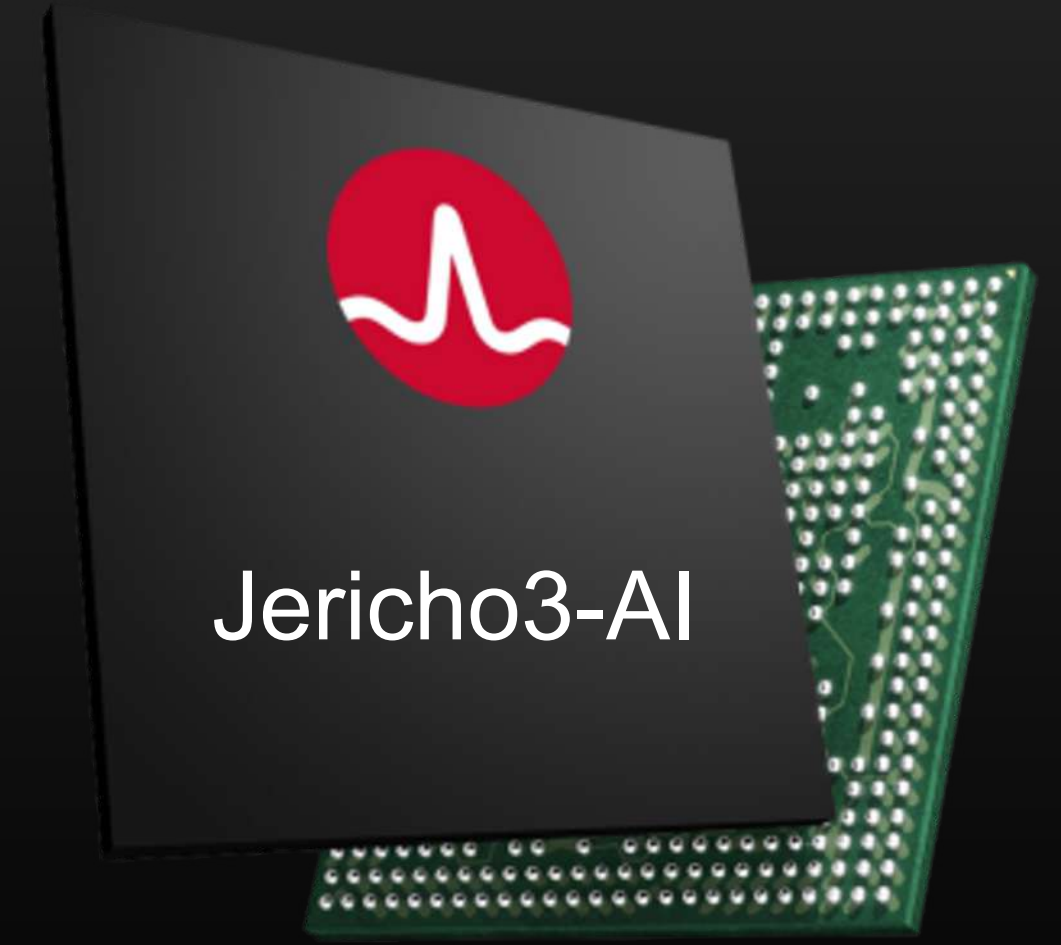
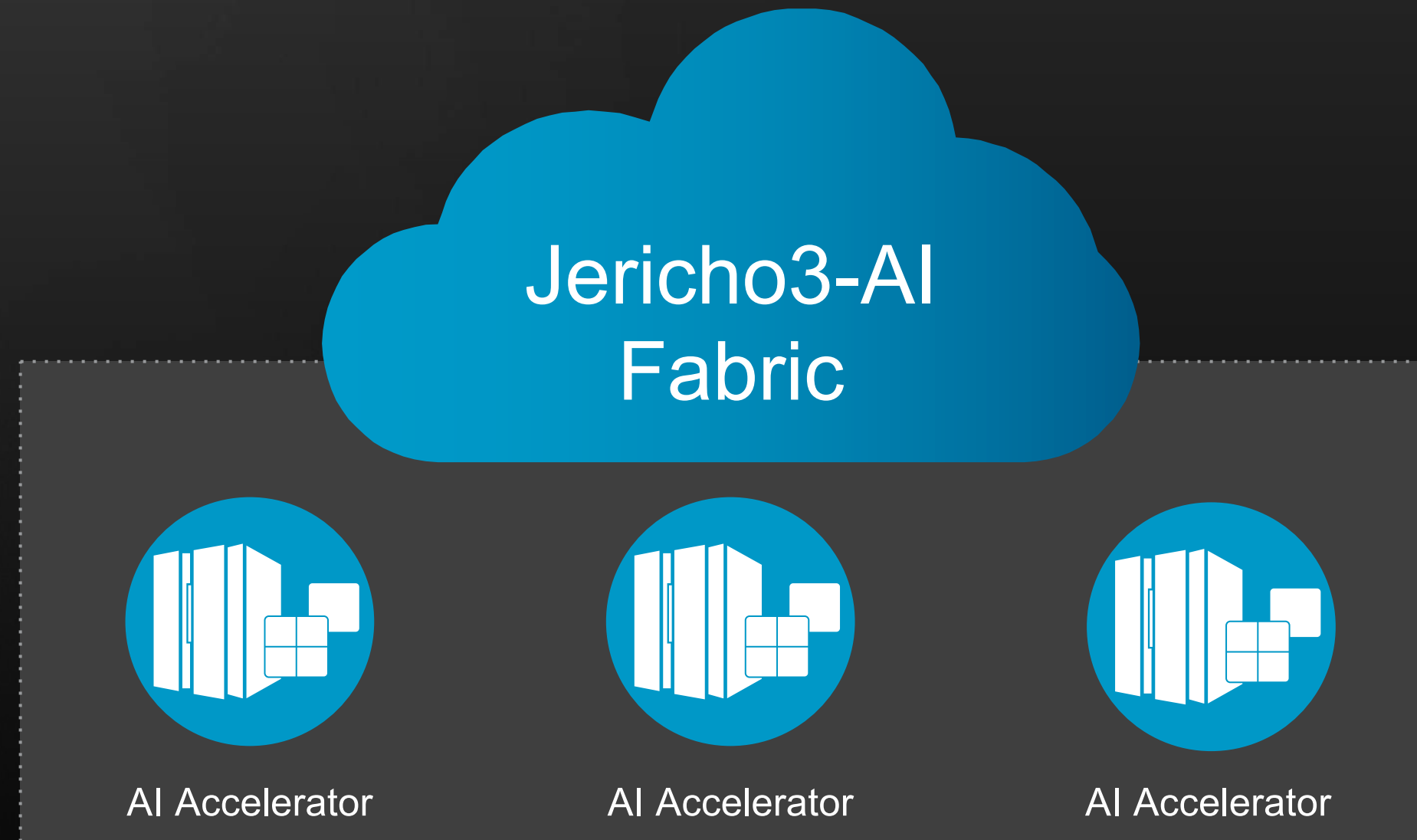
Broadcom's AI Network Solutions



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Jericho3-AI Fabric: Switch Scheduled Ethernet Network

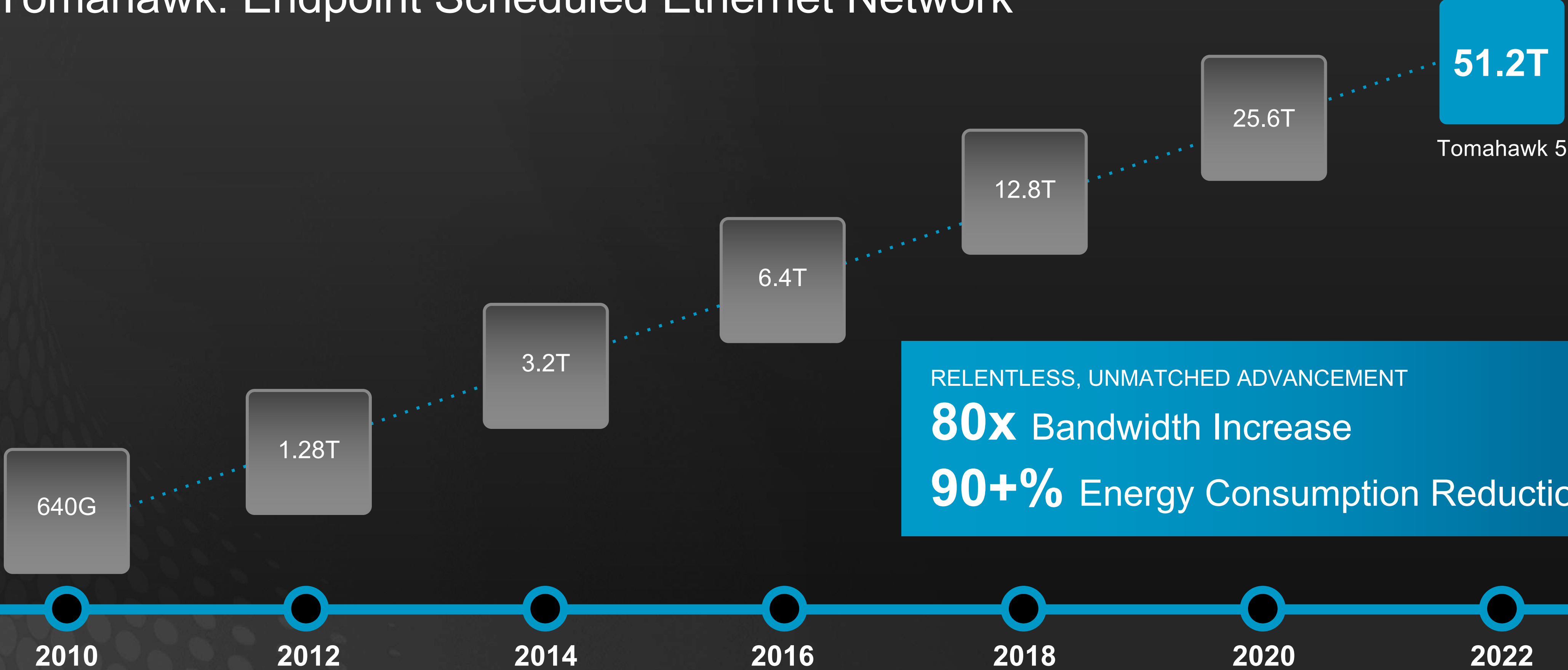
10% Performance improvement = network more than pays for itself



32,000 AI Accelerators at 800Gbps each
Lowest time spent in networking

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Tomahawk: Endpoint Scheduled Ethernet Network



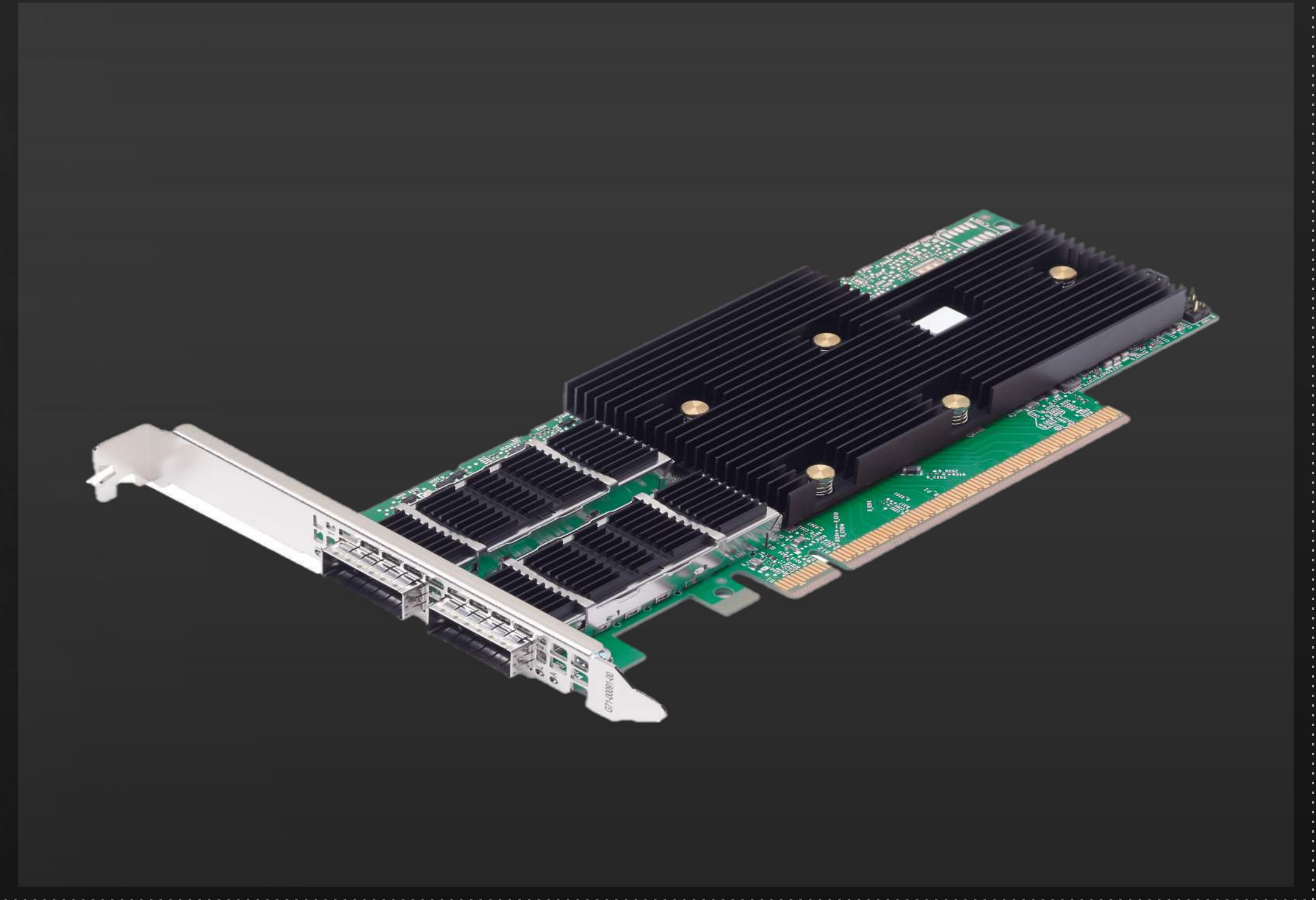
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* G=Gbps, T=Tbps

Introducing Thor2: AI Optimized NIC

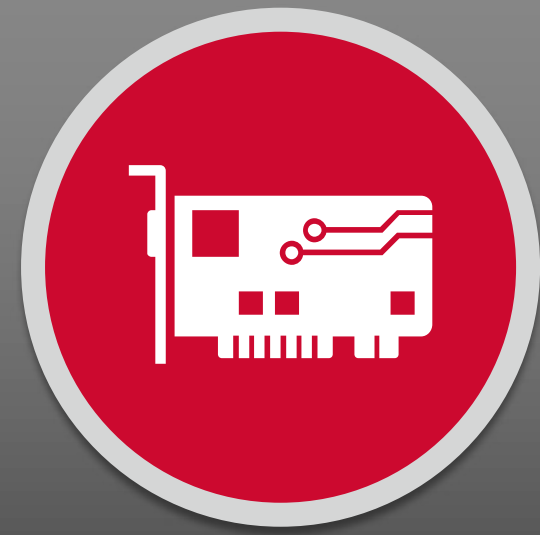
Thor2

- 400G high-performance NIC
- High-scale RDMA
- Industry's lowest power
- Longest reach 100G Serdes

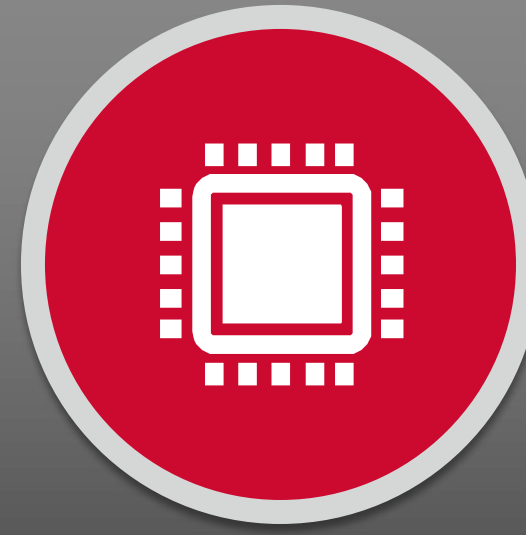


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Thor2 Consumption Models



Board



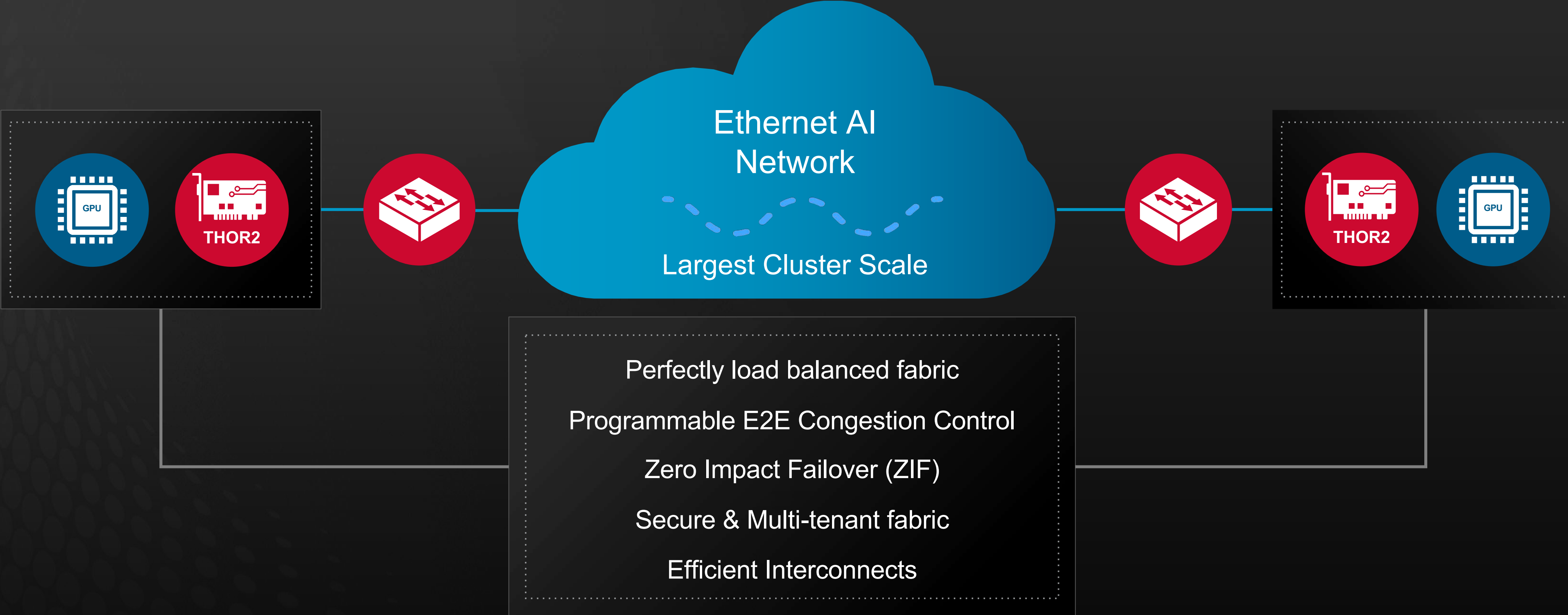
Chiplet



IP

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End-to-End High Performance Ethernet AI Network



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Ethernet Beats InfiniBand: 10+% Improvement in Job Completion Time



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Ethernet Provides 30x Faster Failover than InfiniBand

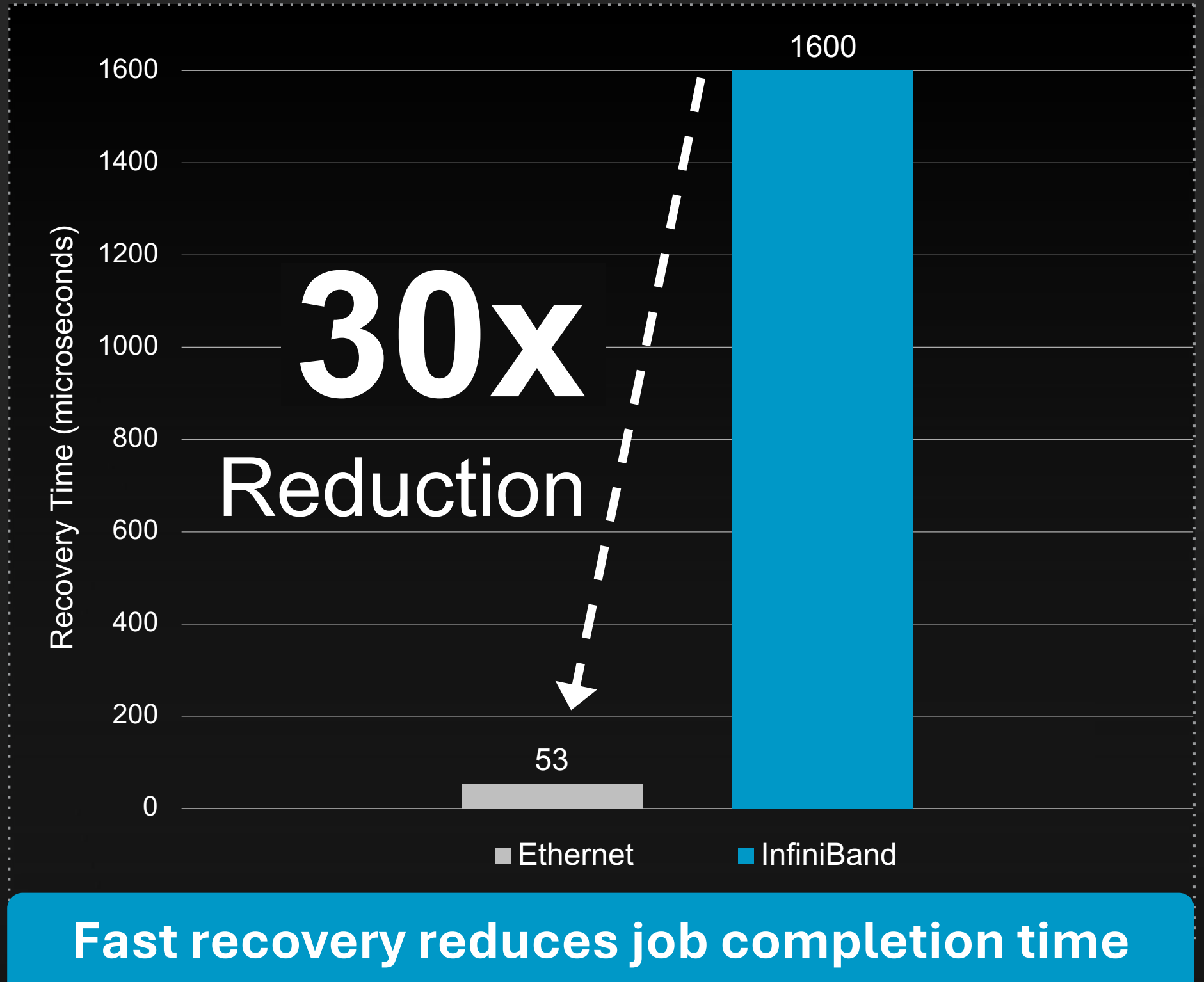
2%

Optics Annual Failover Rate*



15

Failures per Month**



Source: Broadcom Internal Estimates

* Typical industry failure rate. ** Assuming 4K node cluster using 9.2K optic modules

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Reducing AI Interconnect Cost and Power

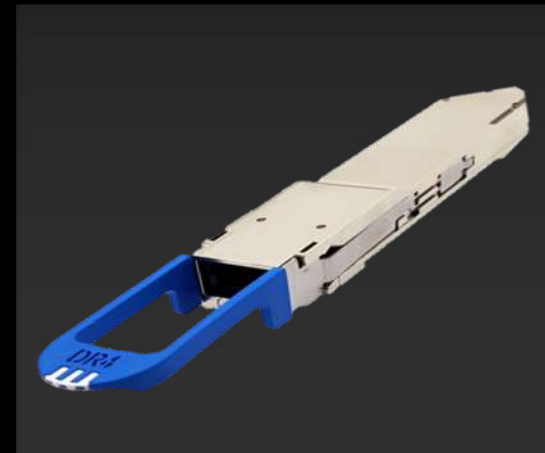
Extended Reach for
Copper Cables

4m+ DAC (2x IEEE spec)



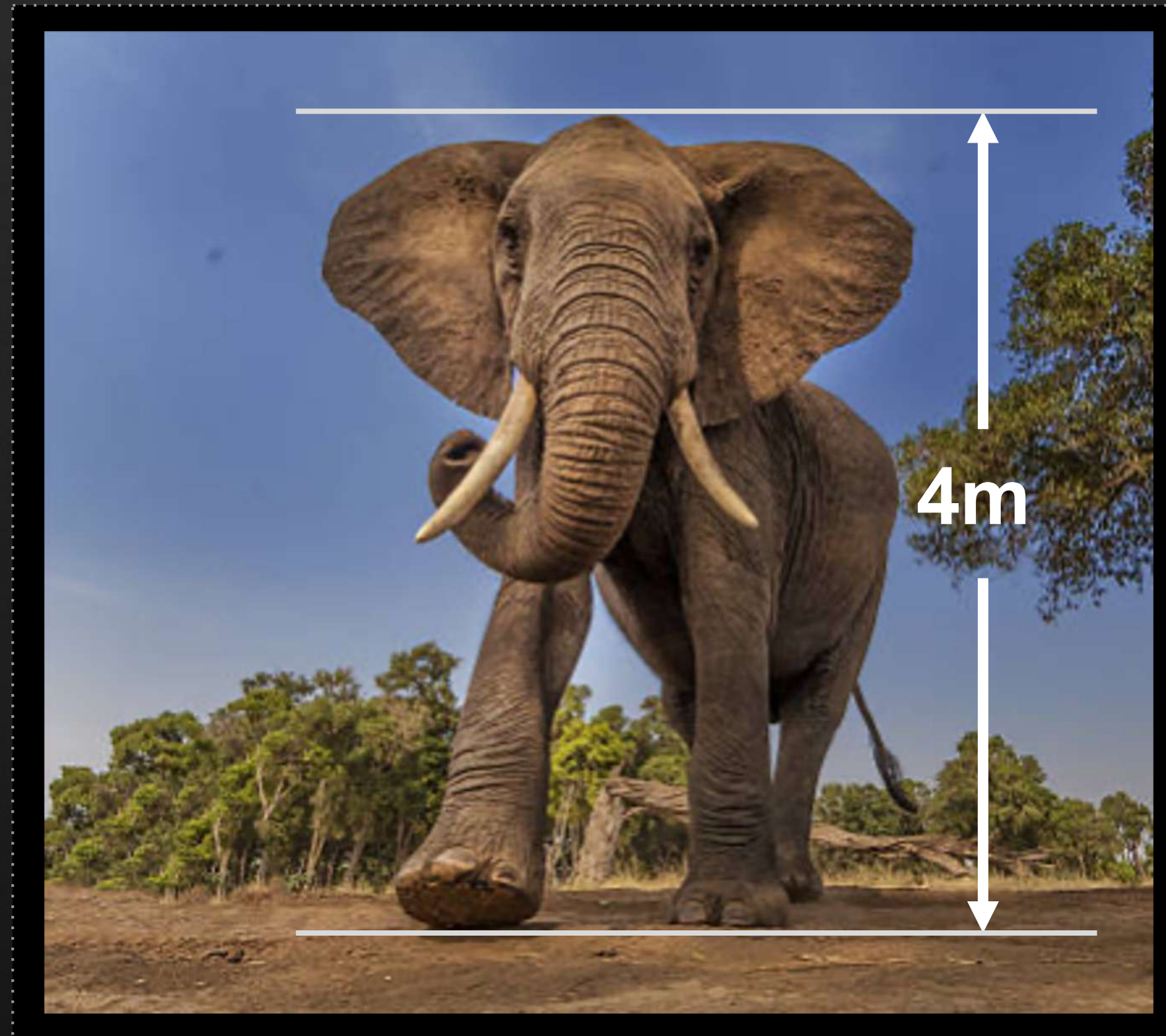
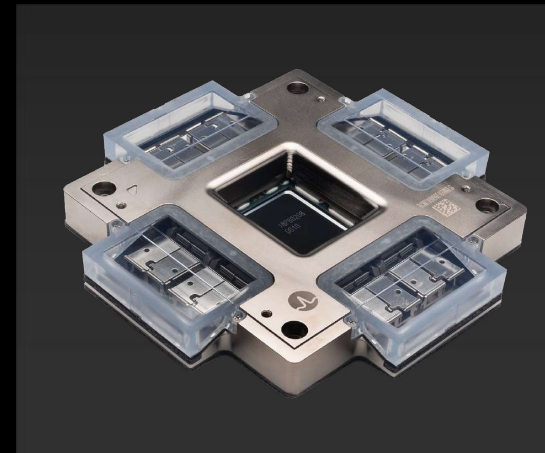
Linear Pluggable
Optics

33% Lower Power



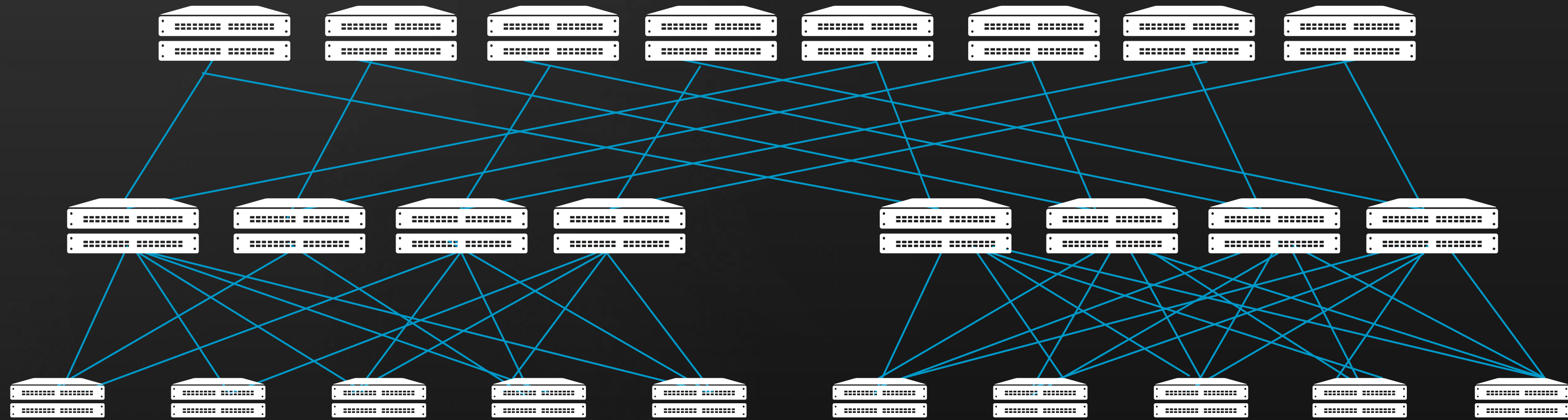
Co-Packaged
Optics

Lowest Power & Cost



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Ethernet is the De-facto AI Network



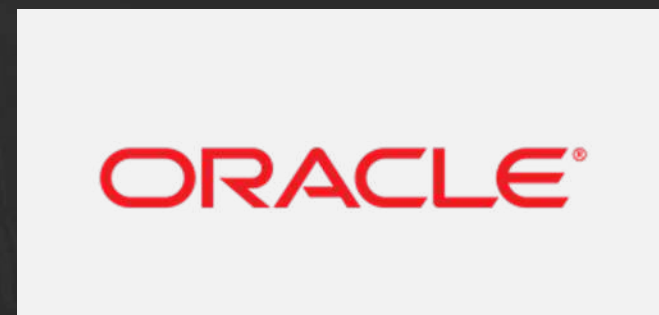
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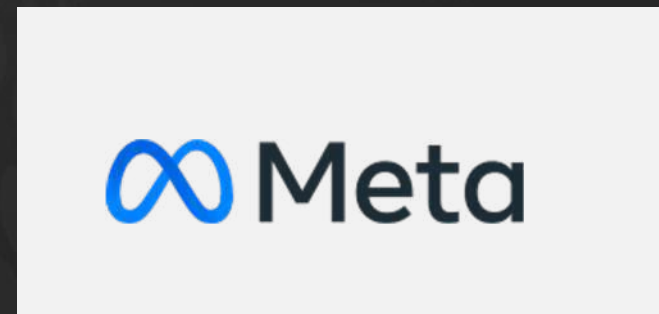
Large Ethernet AI Clusters



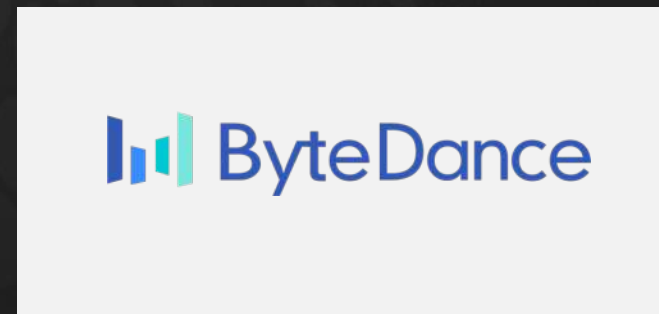
60,000+



30,000+



20,000+



10,000+

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Ultra Ethernet: AI at Scale







Incredibly Strong Industry Reception: 55+ companies

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Modernizing RDMA...

Classic RDMA

-  In-order packet delivery
-  Go-back-n → inefficient
-  No multipathing
-  DCQCN → hard to tune

UltraEthernet

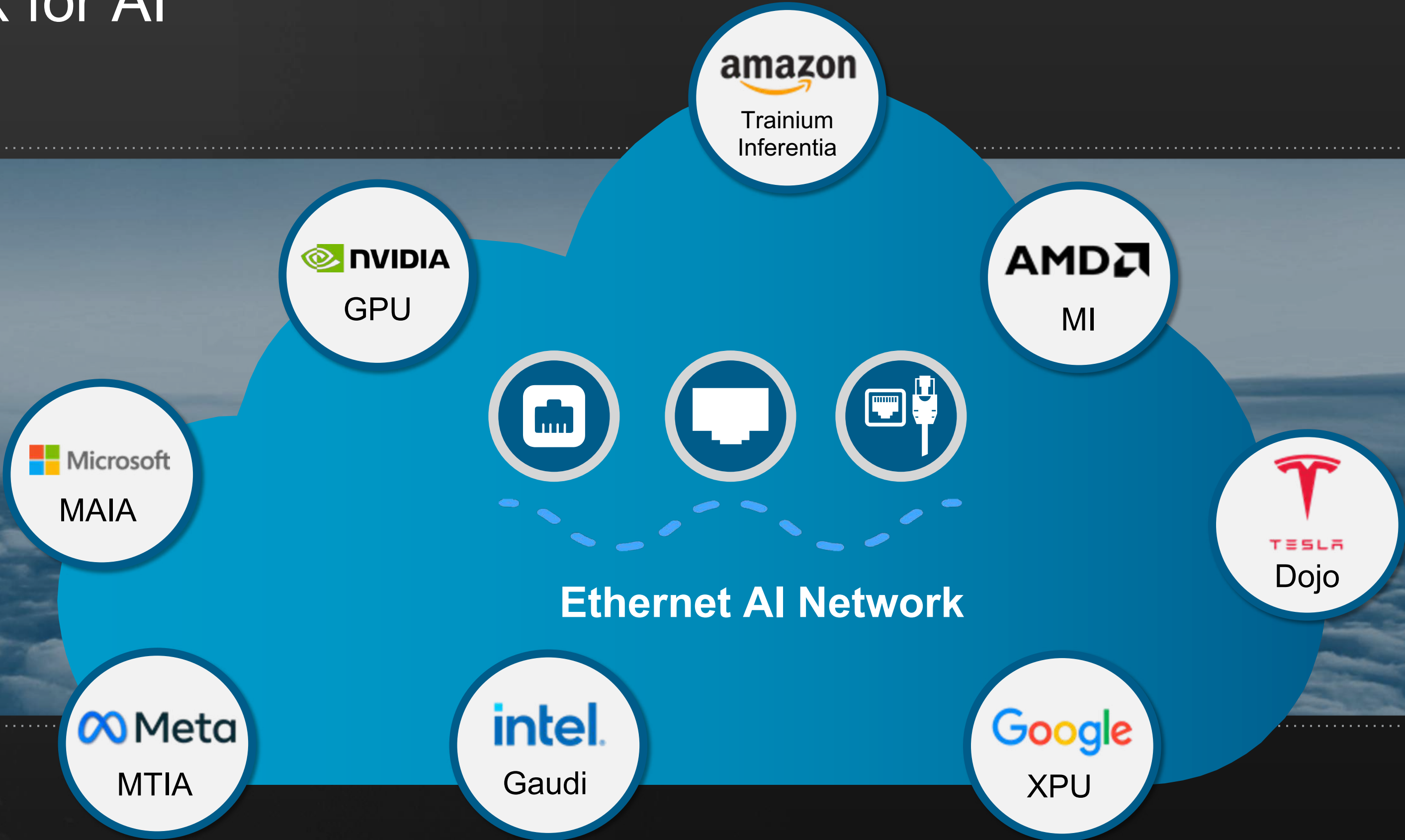
Out-of-order placement,
in-order message completion

Selective Ack and retransmit

Packet-level multipathing

Configuration-free congestion control

Ethernet Network for AI



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Comprehensive Ethernet Portfolio and Ecosystem

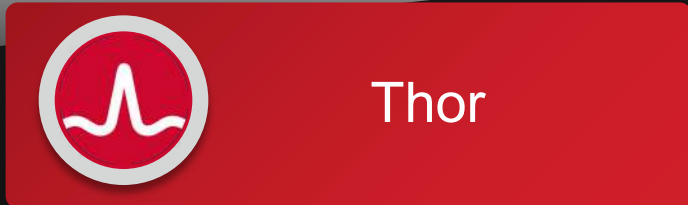
Network Control & Automation



Operation System



Hardware Platform



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AI Server Interconnect

Jas Tremblay
General Manager
Data Center Solutions Group
Broadcom



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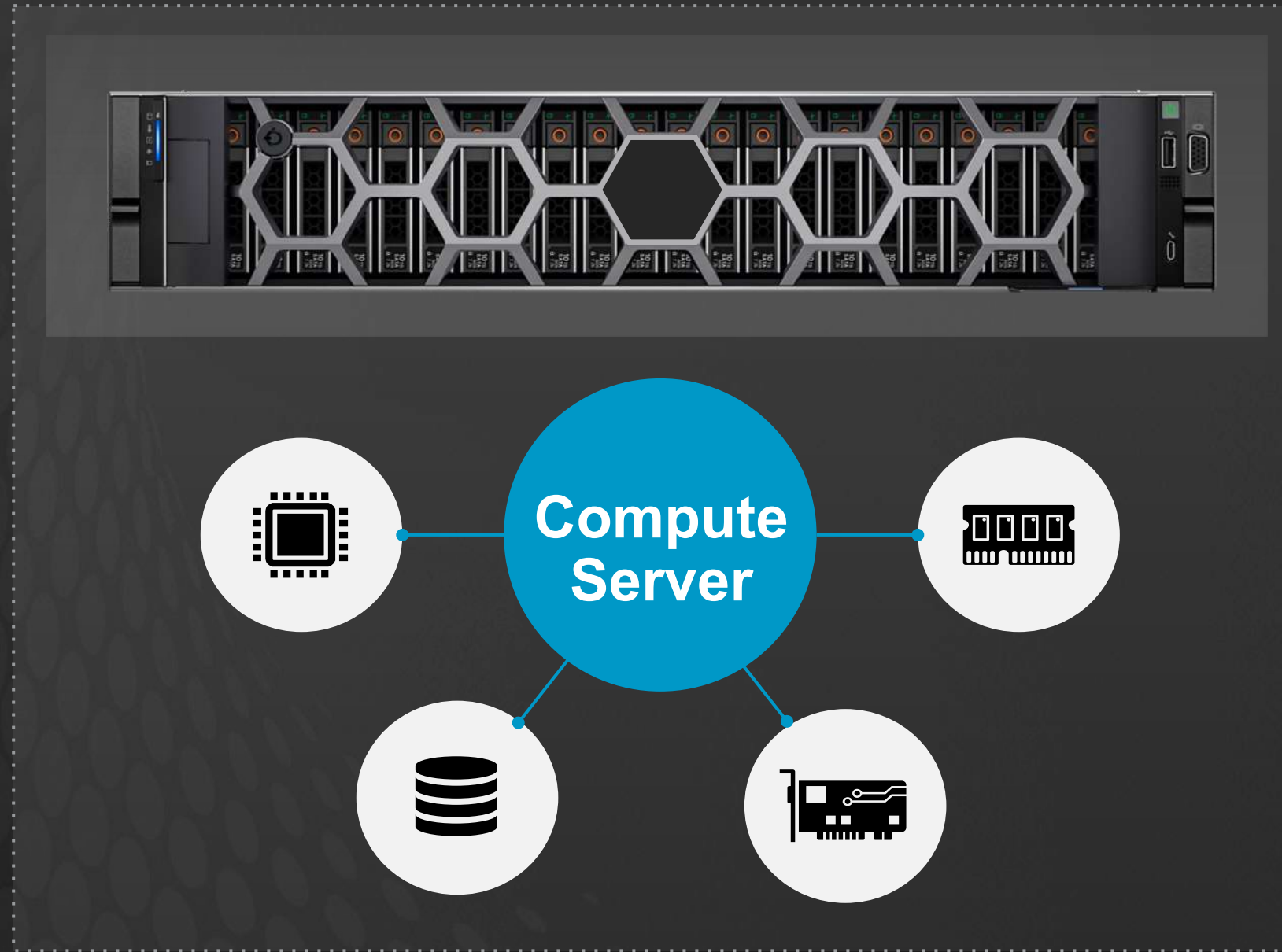
Server Interconnect History



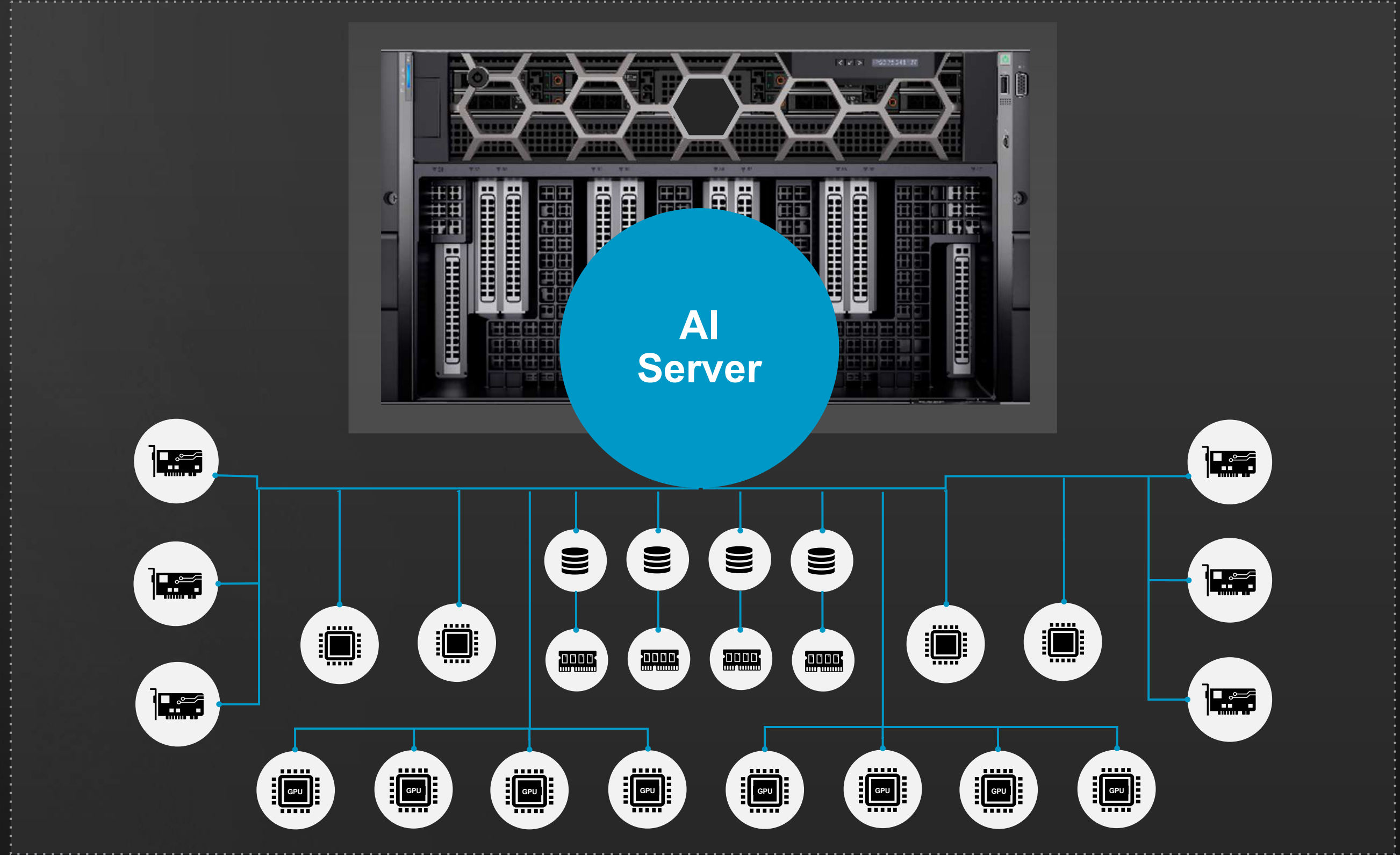
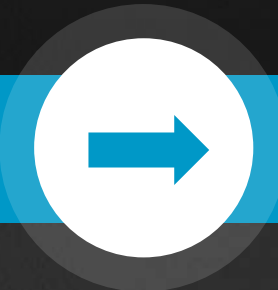
PCI Standards Group: Founded in 1992 with 900+ Companies

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Server Evolution



Compute Centric



High-Performance Interconnect

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AI Server: Open → Options

Accelerators



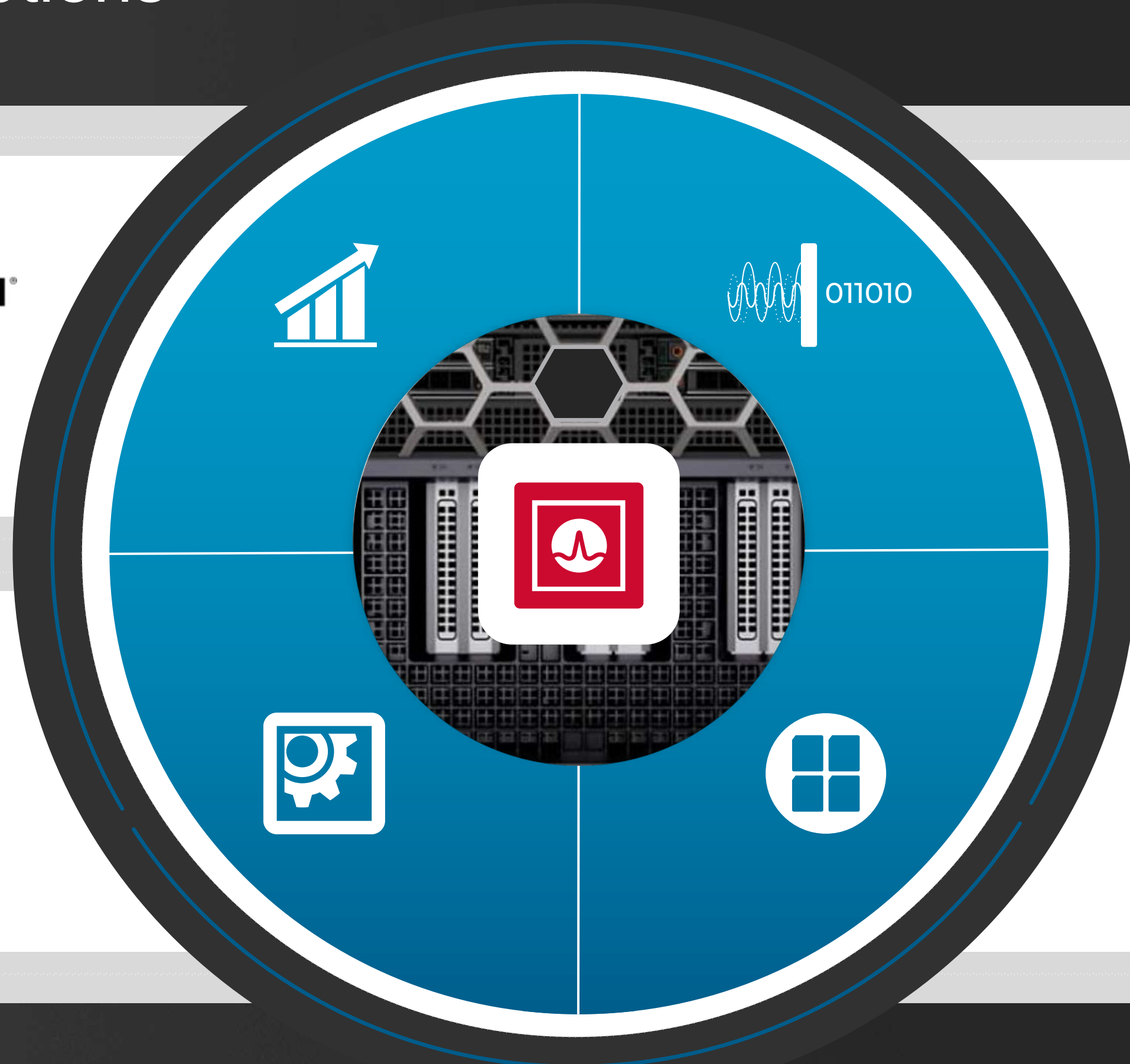
Central Processing Unit



NIC

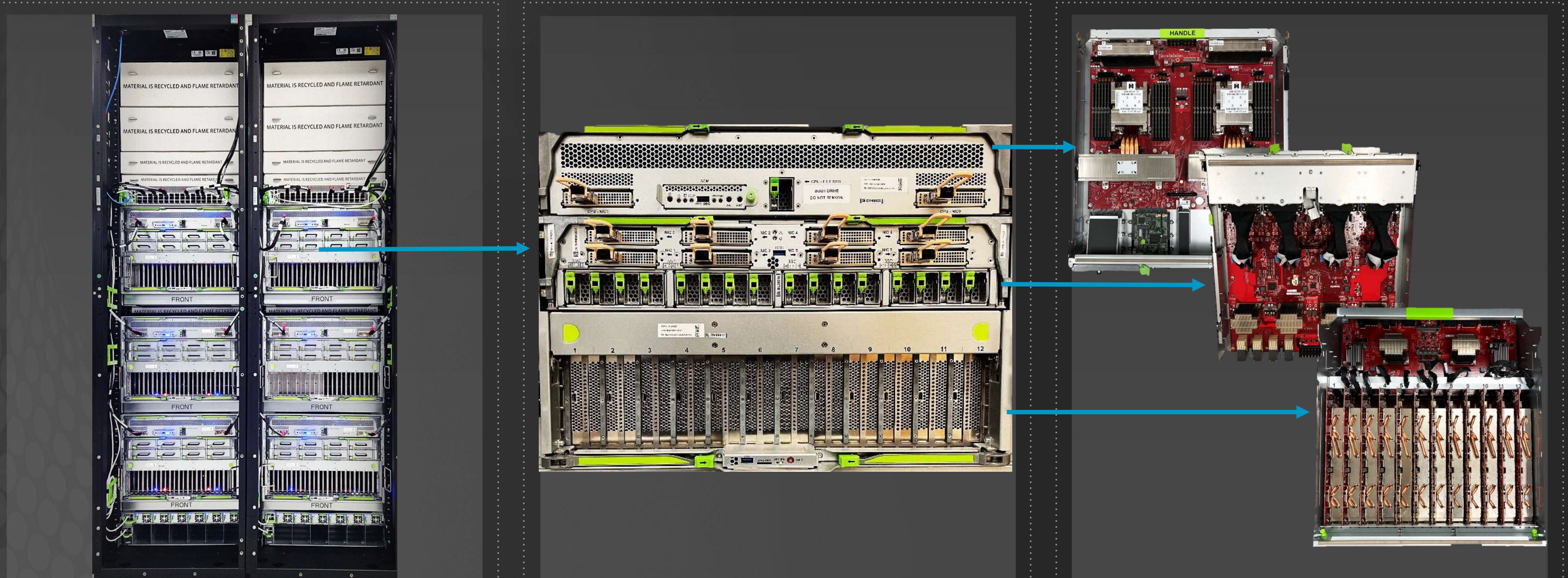


Storage & Memory



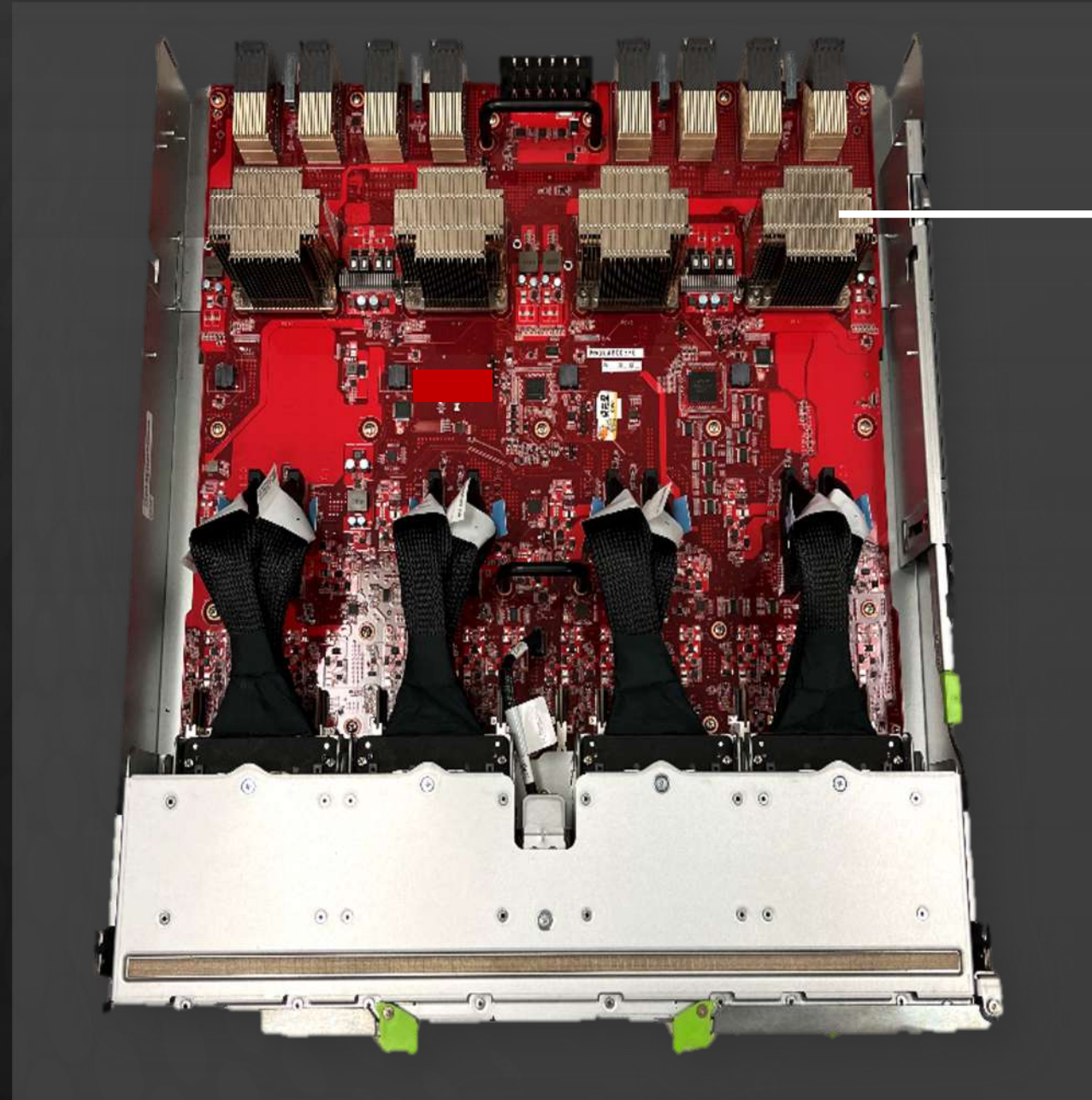
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AI Rack: Interconnect



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AI Server: Interconnect

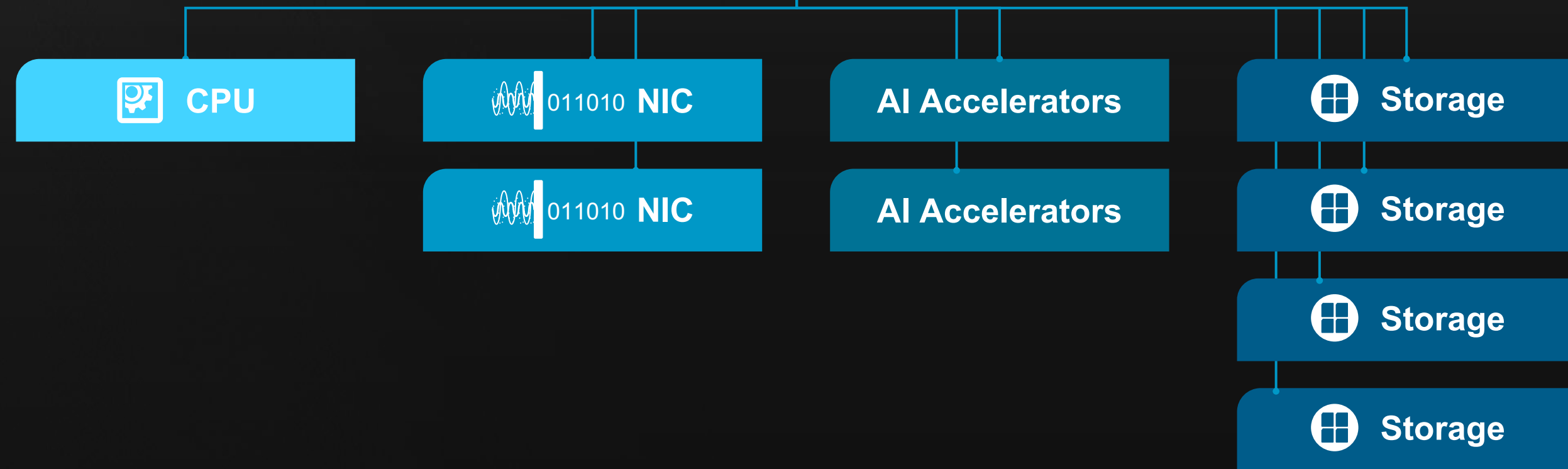


4x



PCIe Switch

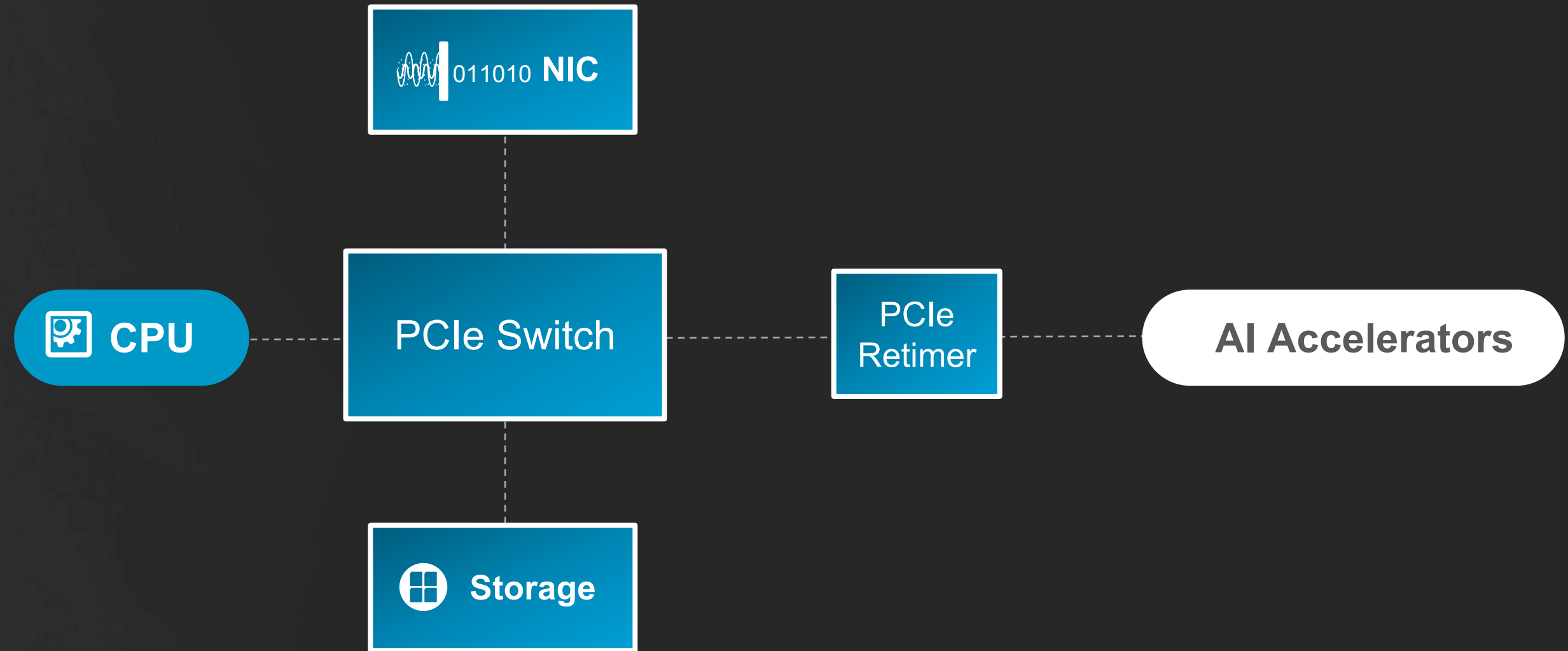
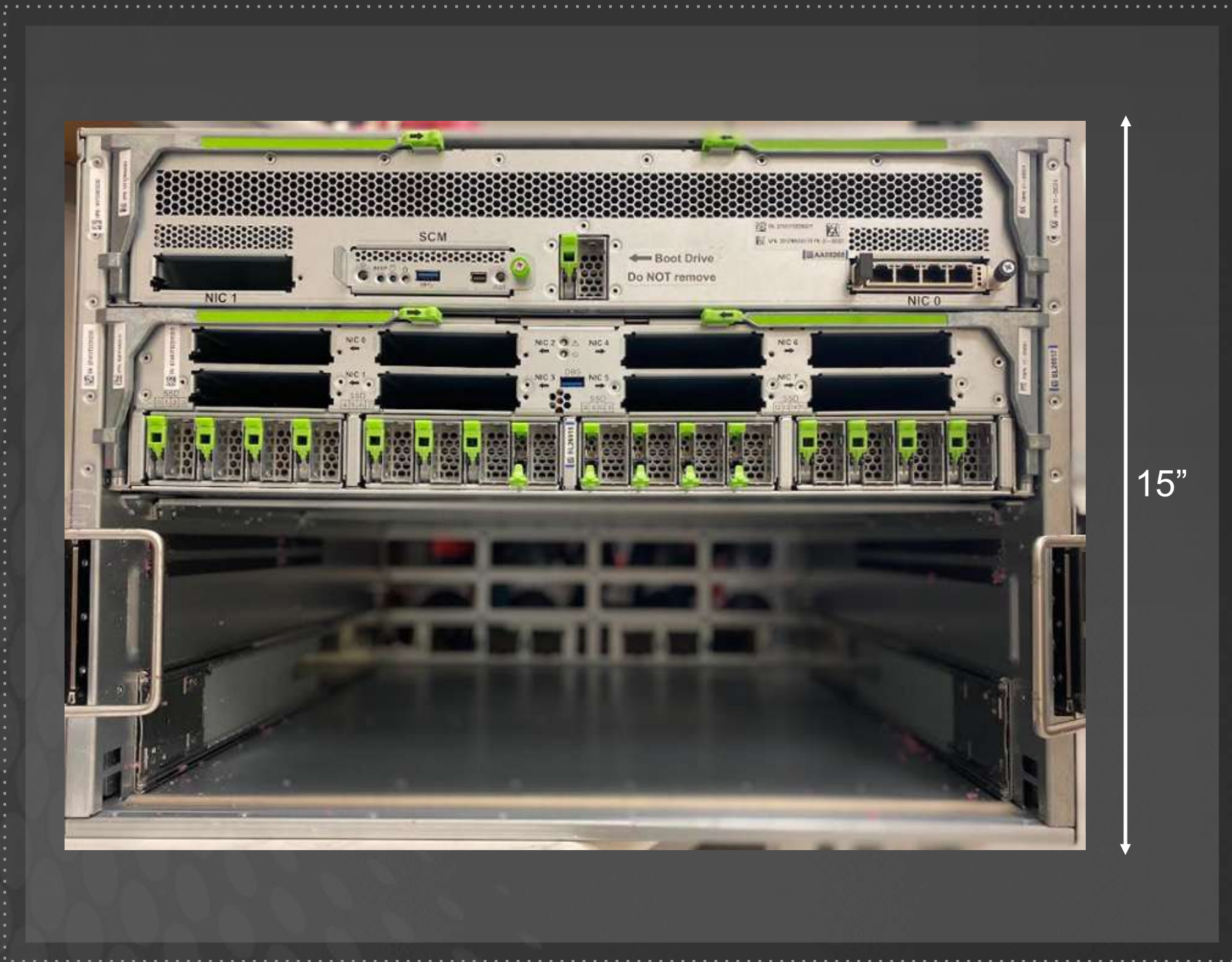
- 144 lanes
- PCIe Gen 5
- 120 nanosec latency



Most Trusted PCIe Device

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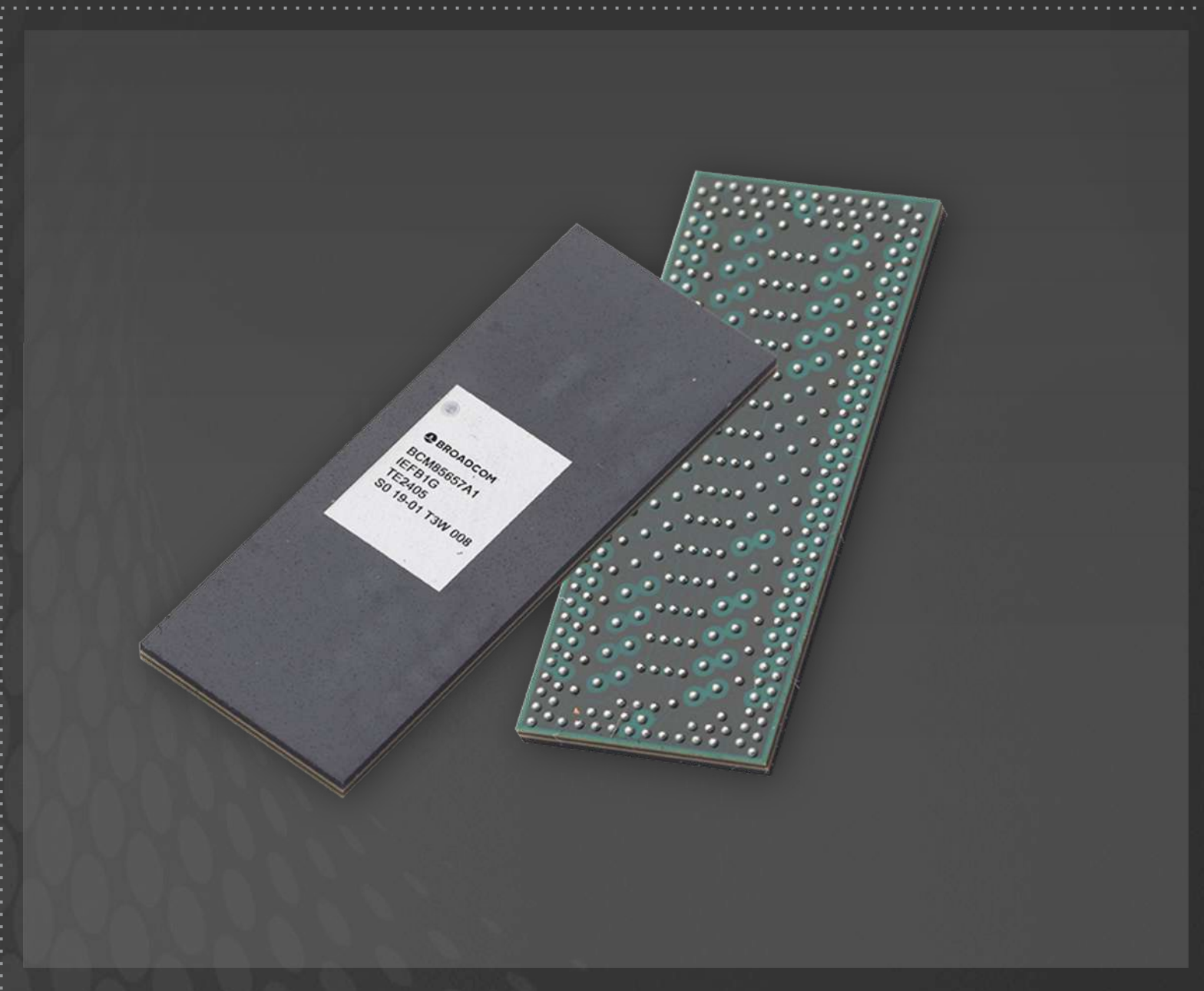
AI Server: PCIe Interconnect



End-to-End AI PCIe Connectivity

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AI Server: PCIe Retimer



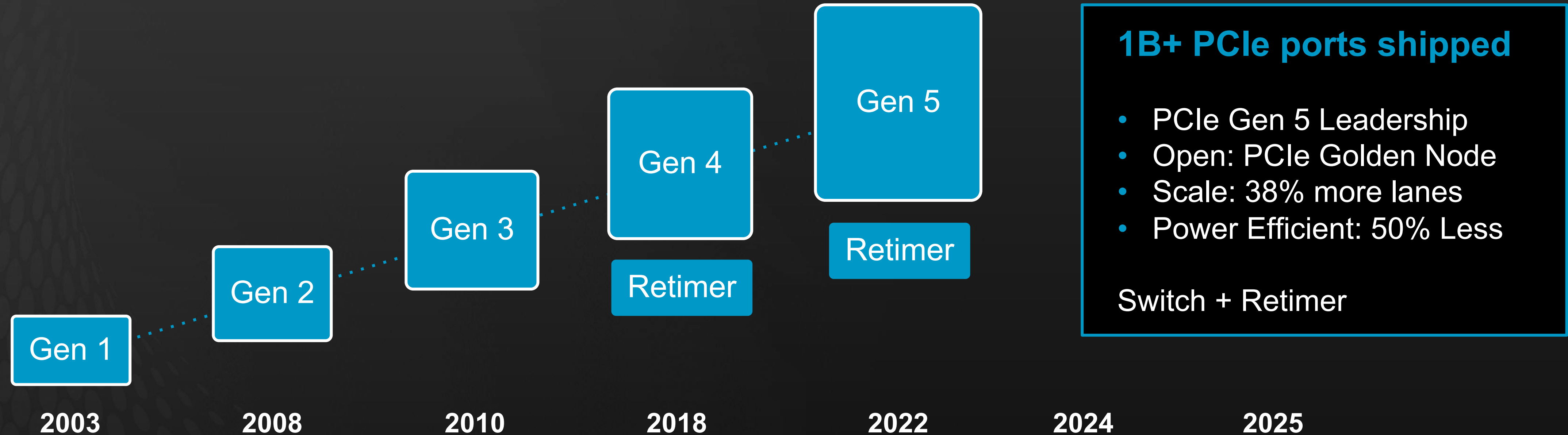
Retimer	Competition	Broadcom
Technology	7 / 16nm	5nm
SerDes	Third Party	In House
Power	1x	35% Less
Reach	1x	40% More

Source: Broadcom Internal Estimates

End-to-End AI PCIe Connectivity

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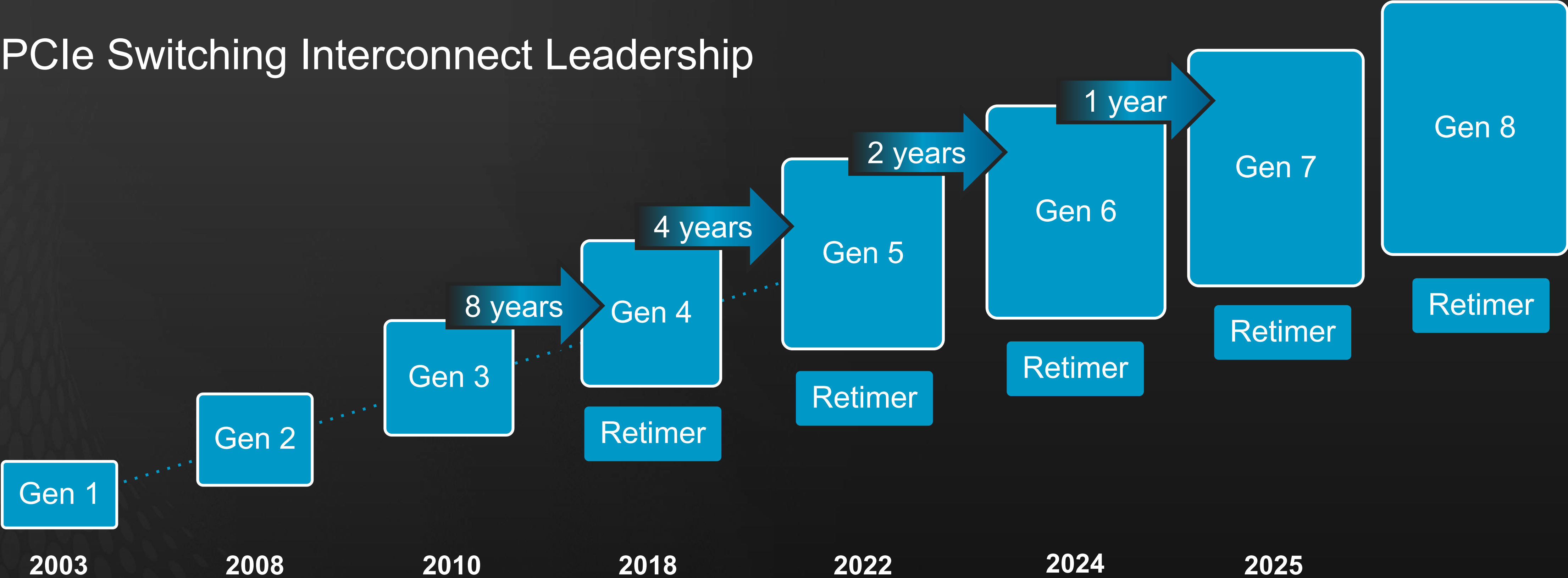
PCIe Switching Interconnect Leadership



First to Market for 20 Years ... 5 Successful Generations

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PCIe Switching Interconnect Leadership



Accelerating PCIe Switch + Retimer Introduction

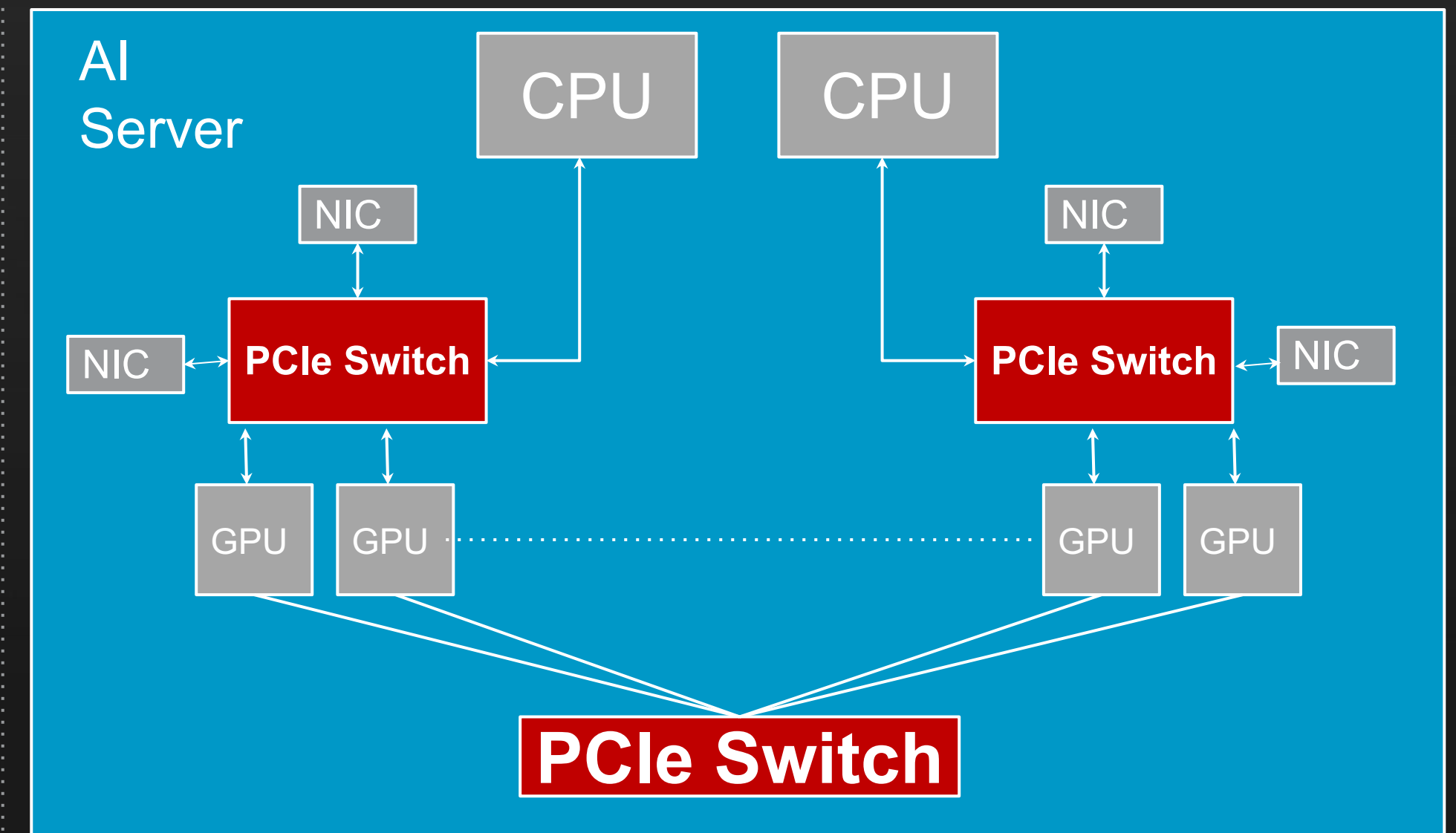
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AI Server: Scale Up



PCIe Gen 7 Switch

- Accelerator Fabric Link Latency: ~120 nanosecond
- Scale: Hundreds of Nodes



Scale Up

AMD/Broadcom Collaborate on Scale Up Fabrics

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AI Server Connectivity

Key Points



PCIe is key to AI Server **OPEN** interconnect



Decades of market leadership in **SCALABLE** PCIe Switches and Retimers



Broadcom end to end PCIe delivers 40% greater reach with 50% lower **POWER**

Source: Broadcom Internal Estimates

OPEN // SCALABLE // POWER EFFICIENT

ENABLING AI Infrastructure

Optical Interconnects

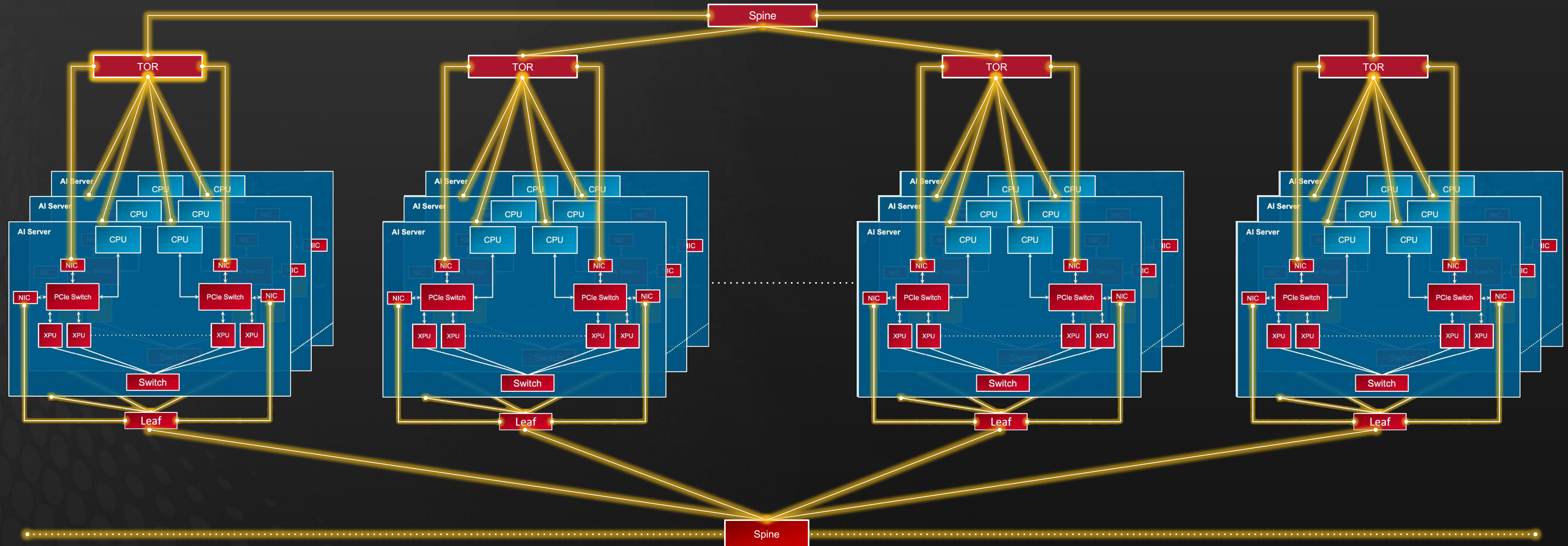
Near Margalit, Ph. D.

General Manager
Optical Systems Division
Broadcom



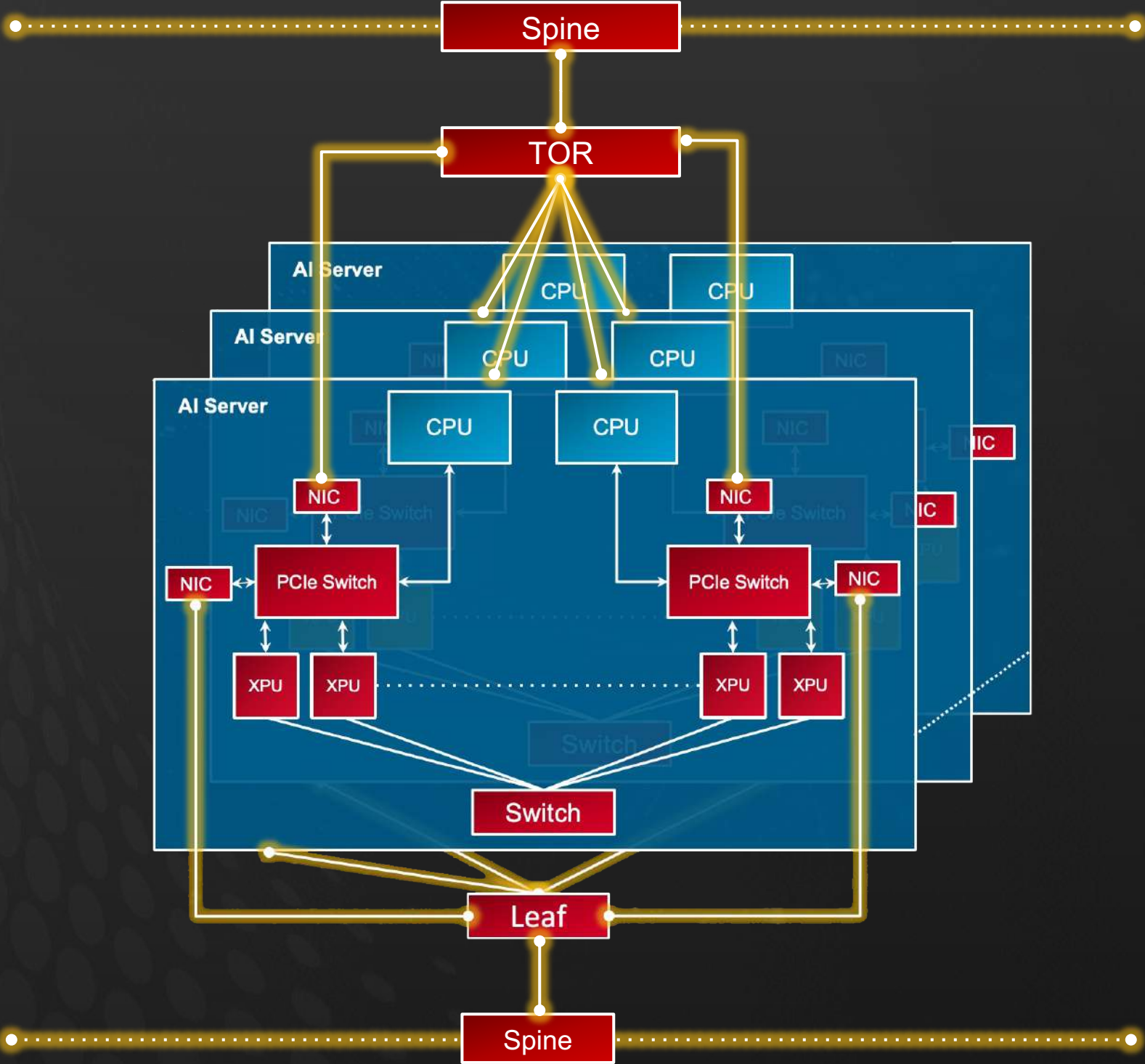
OPEN // SCALABLE // POWER EFFICIENT

The Optical Interconnect for AI



OPEN // SCALABLE // POWER EFFICIENT

Optical Interconnect for AI



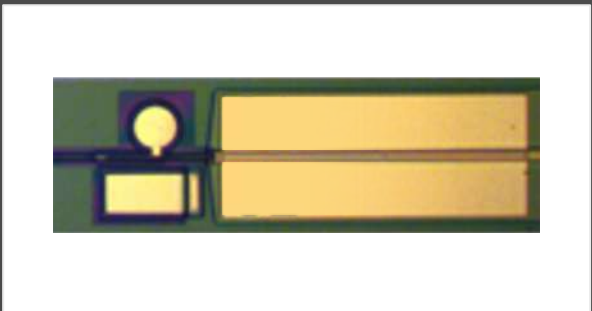
#1



VCSEL

Multi-mode, short reach

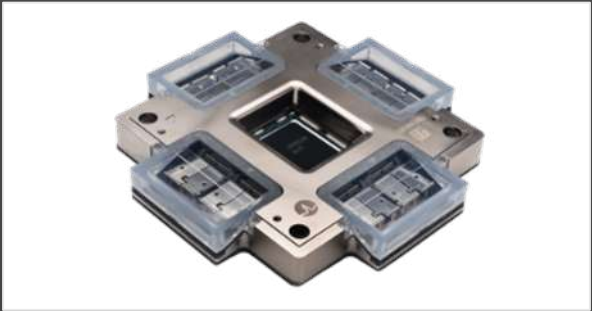
#1



EML

Single-mode, long reach

1st

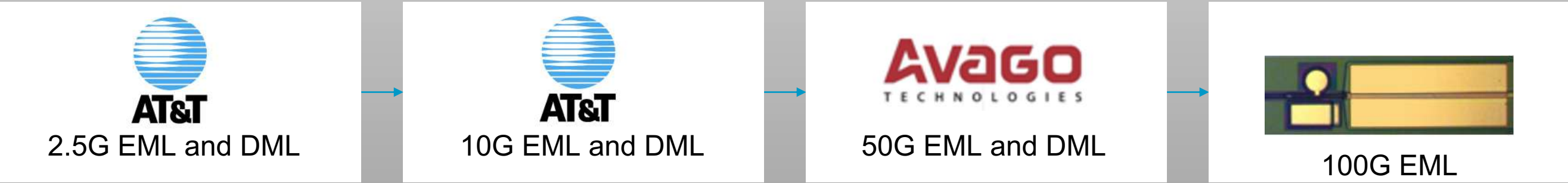


CPO
(SiPho)

Power and cost leadership

OPEN // SCALABLE // POWER EFFICIENT

Broadcom Optics Leadership

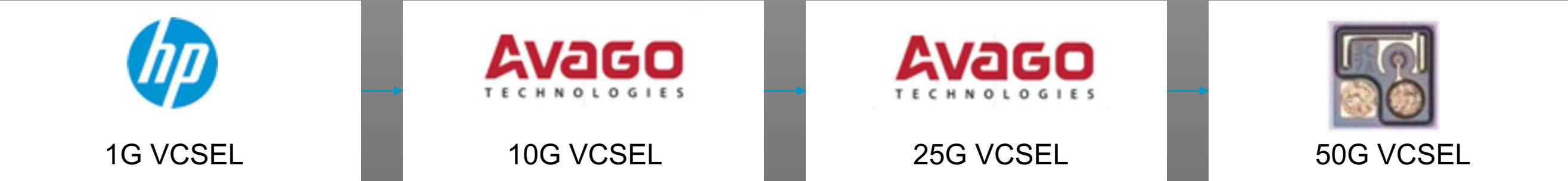


50M+

High-Speed Communication Lasers Shipped Annually

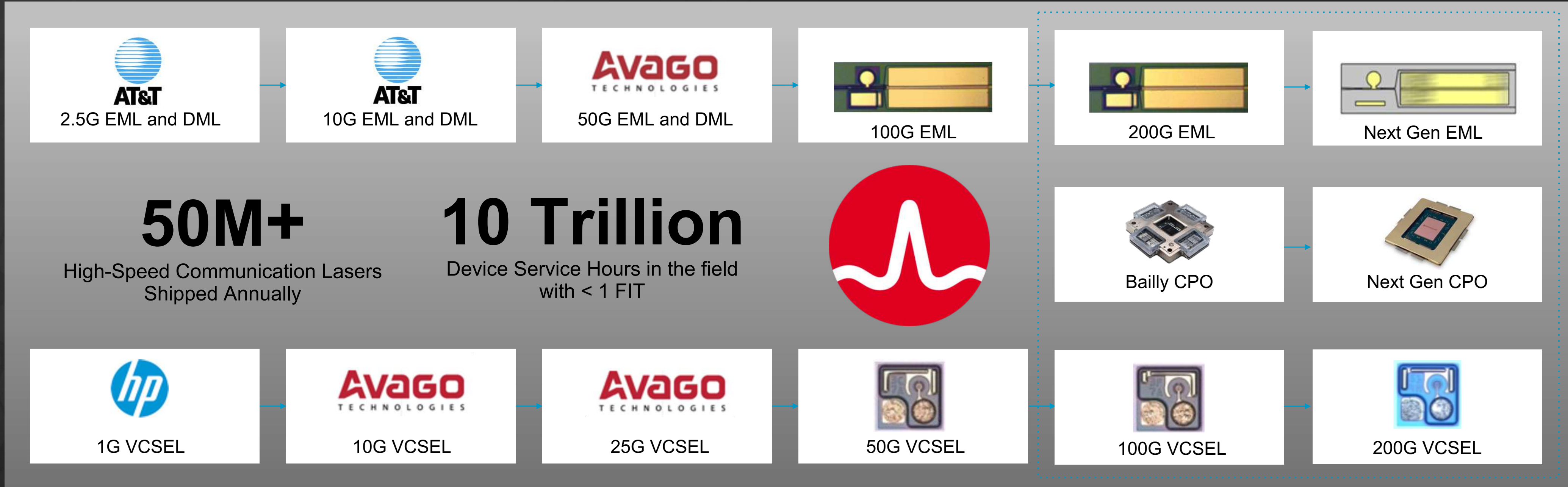
10 Trillion

Device Service Hours in the field with < 1 FIT



OPEN // SCALABLE // POWER EFFICIENT

Broadcom Optics Leadership



1998 2004 2013 2019 2023 2025

OPEN // SCALABLE // POWER EFFICIENT

Why Co-Packaged Optics (CPO)?



Lowest Cost/Bit

Massive reduction in components and interconnects



Power/Performance Leadership

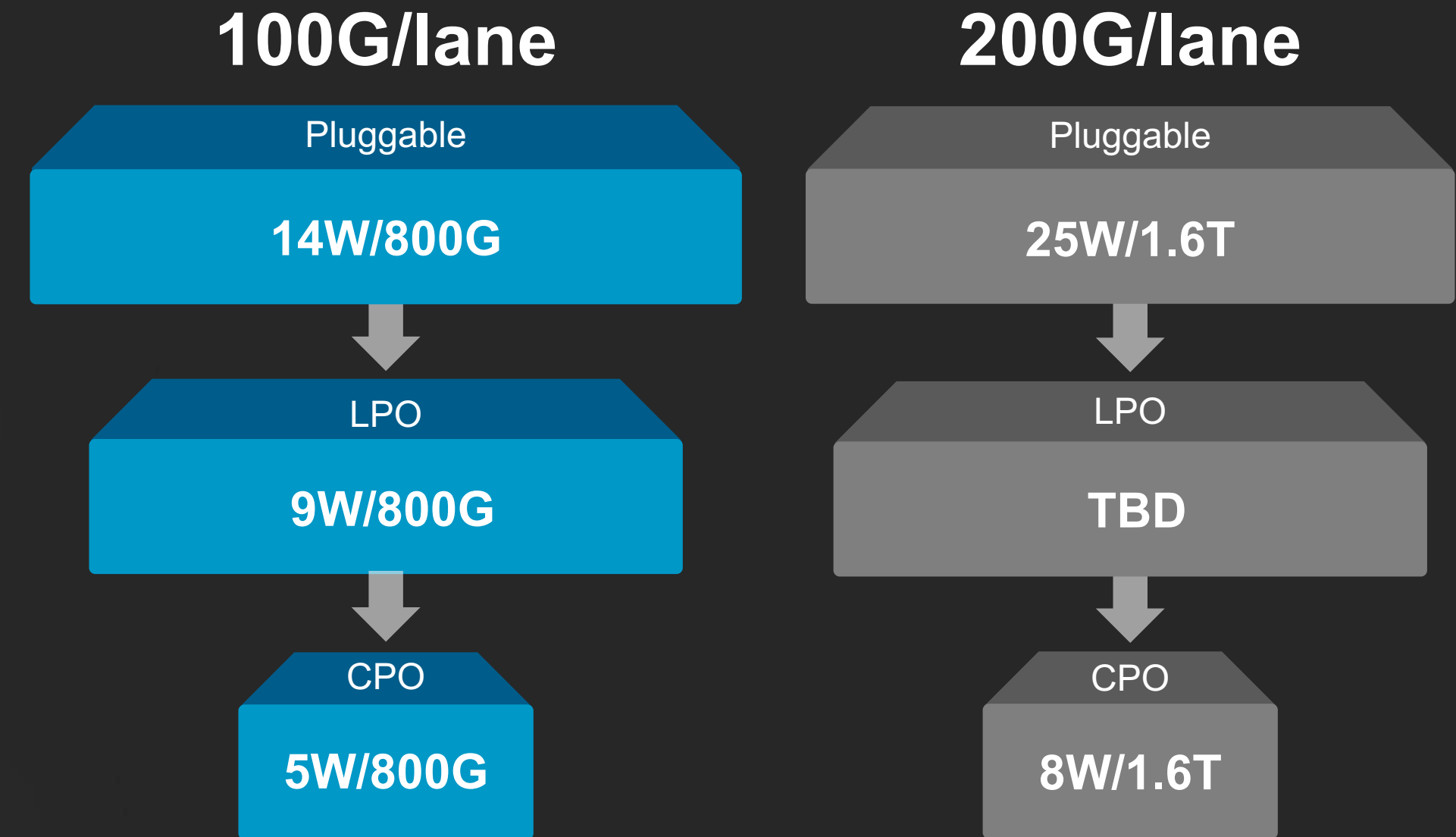
Eliminate electrical interconnect power



Increased Reliability

Silicon integration with pluggable Laser

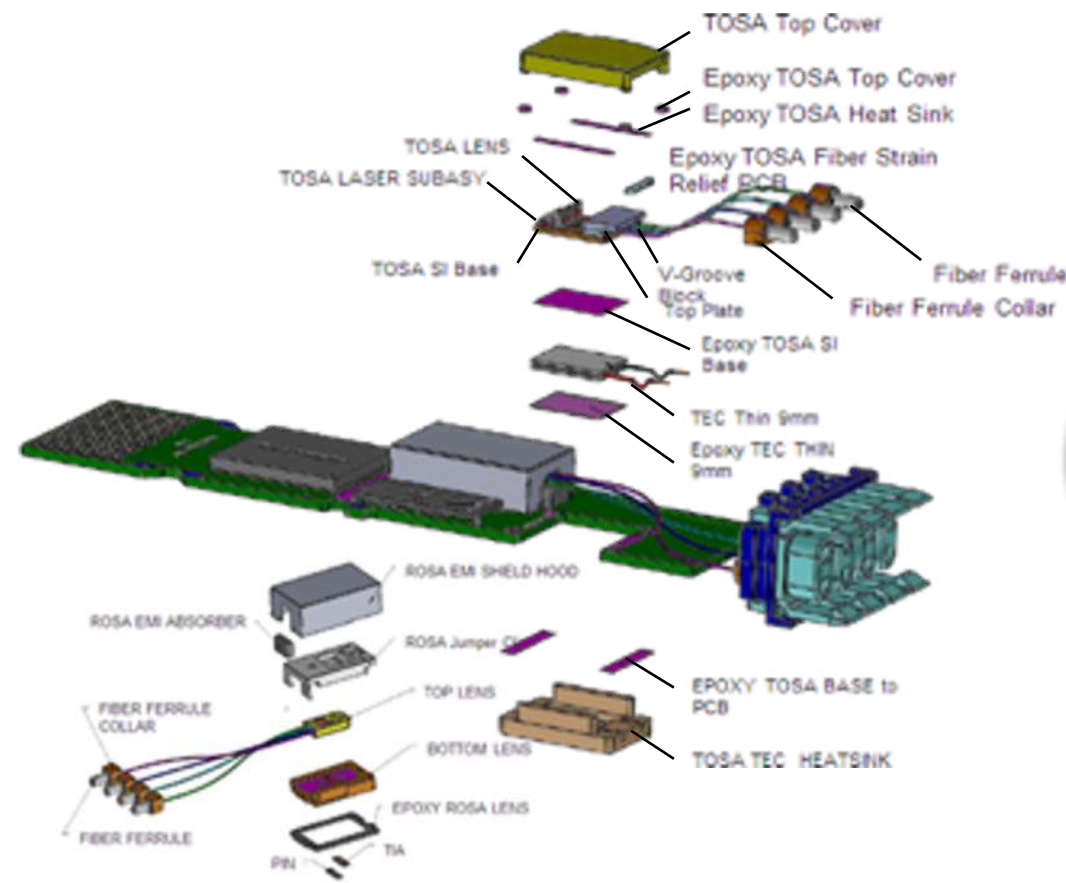
POWER COMPARISON



OPEN // SCALABLE // POWER EFFICIENT

The Journey to Integration at Scale

Conventional Module Design

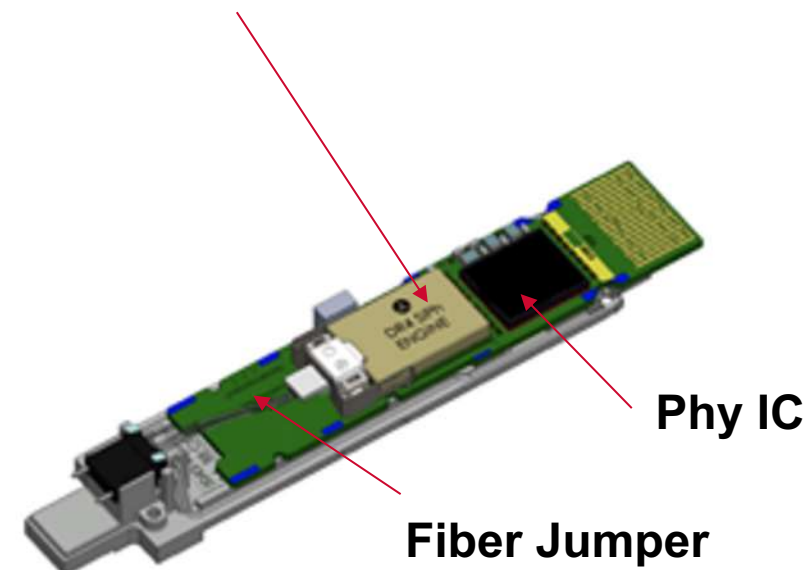


Engineering and manufacturing limits to scale



Integrated SiPh Module Design

SiPh Chipllets in Package (SCIP)

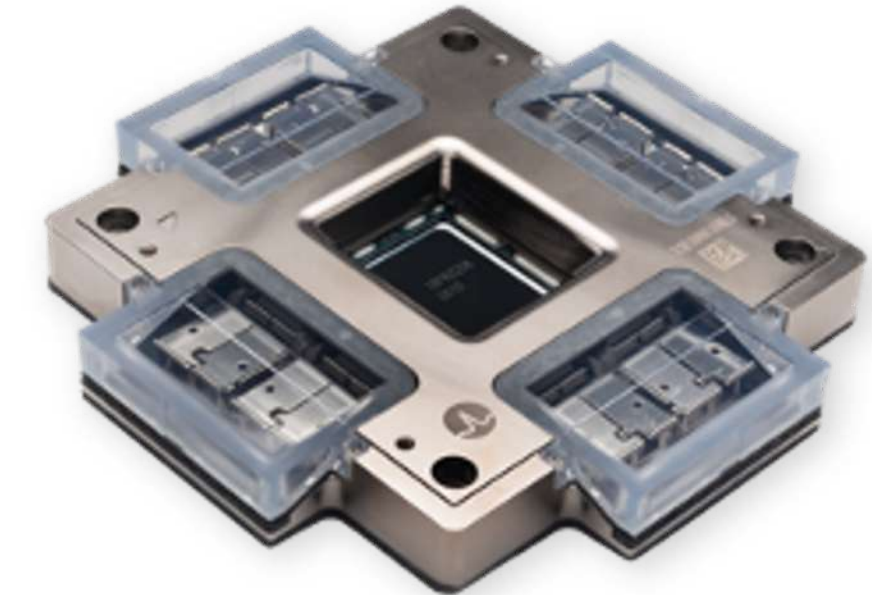


30% fewer piece parts

Module Integration = First step to improved scale



Co-Packaged Optics



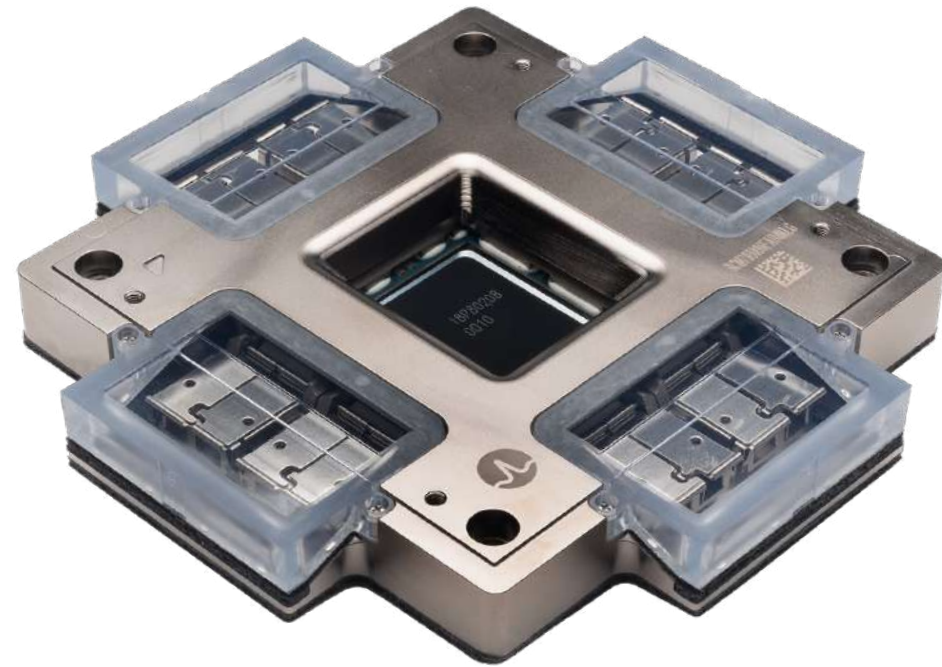
Highly Integrated Optical Engines (up to 6.4T)

FIRST to Productize High-Density Photonic Integration

OPEN // SCALABLE // POWER EFFICIENT

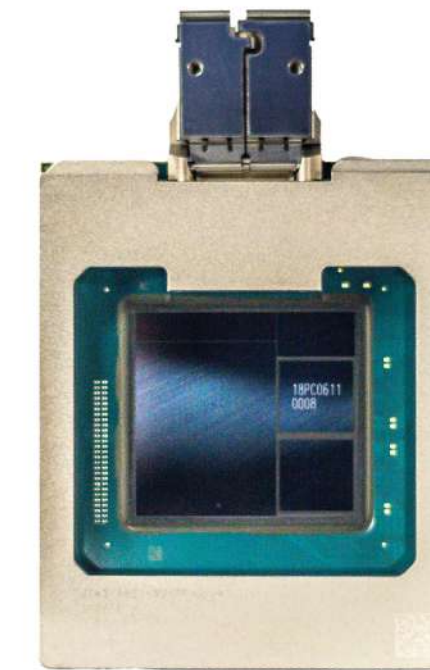
CPO Applications: Ethernet Switch, XPU Interconnect

Ethernet Switch



More than 50Tbps optical connectivity co-packaged with an Ethernet Switch

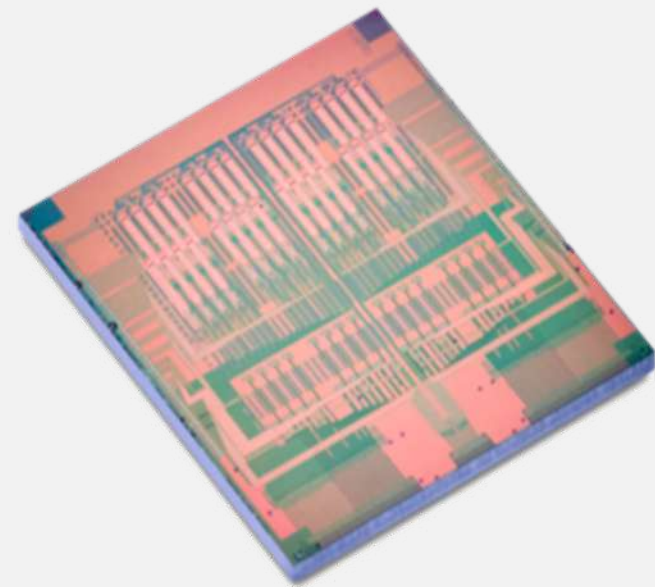
XPU Interconnect



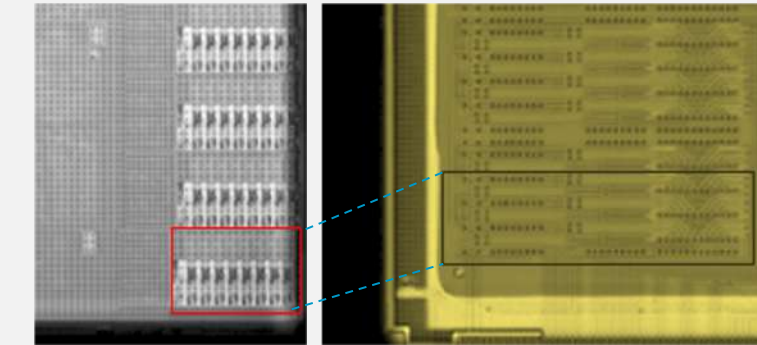
Up to 50Tbps optical connectivity co-packaged with a XPU

OPEN // SCALABLE // POWER EFFICIENT

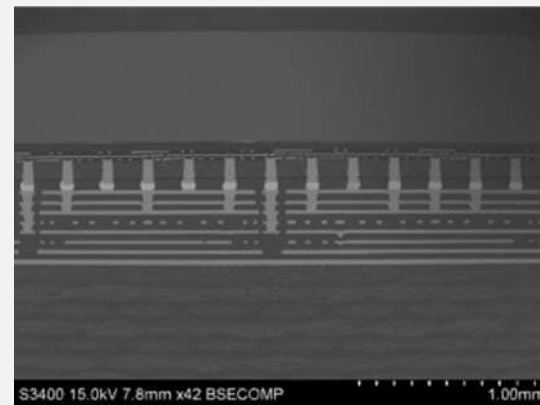
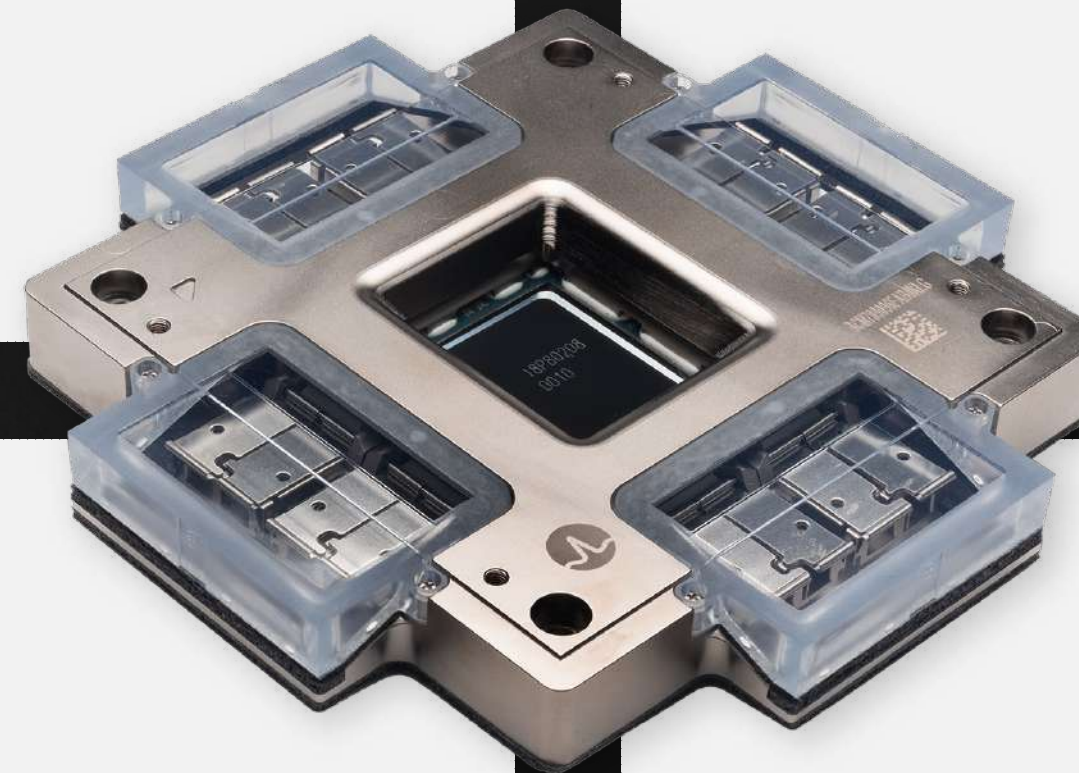
51.2T TH5-Bailly CPO available today



**64 Channel FR4 PIC
with Integrated
Mux/Demux**



**64 Channel
EIC with CMOS
Driver and TIA**



**Advanced
Packaging**

**ODM System
Integration**



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Optical Interconnects

Key Points



Industry leadership on **100G → 200G VCSEL** and **EML**



First commercial **CPO** with pluggable lasers



Unmatched **>70%** power reduction* and **>30%** cost savings

*Source: Broadcom Internal Estimates

OPEN // SCALABLE // POWER EFFICIENT

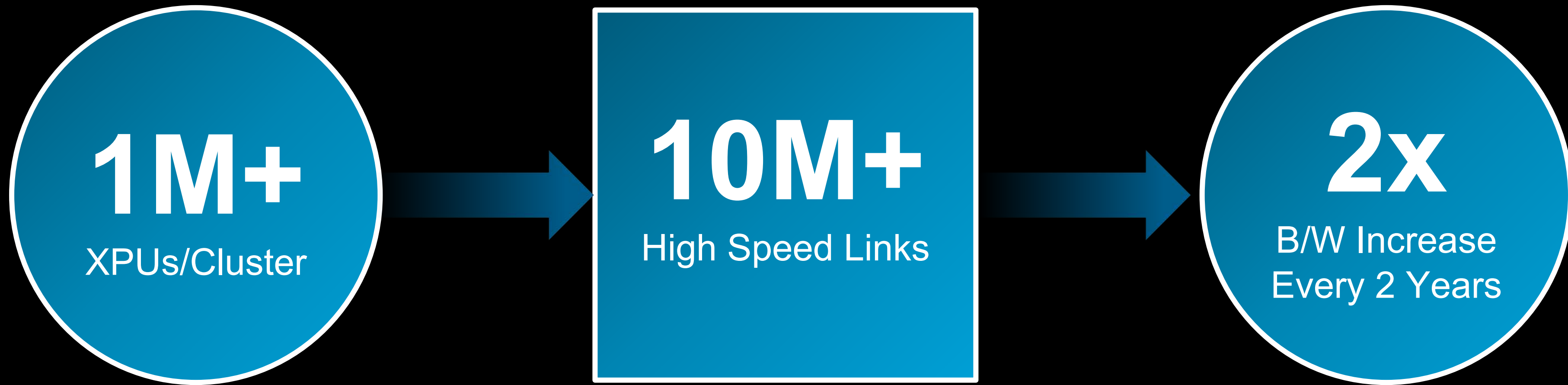
ENABLING AI Infrastructure

**Foundational Technology
for AI Interconnect**

Vijay Janapaty

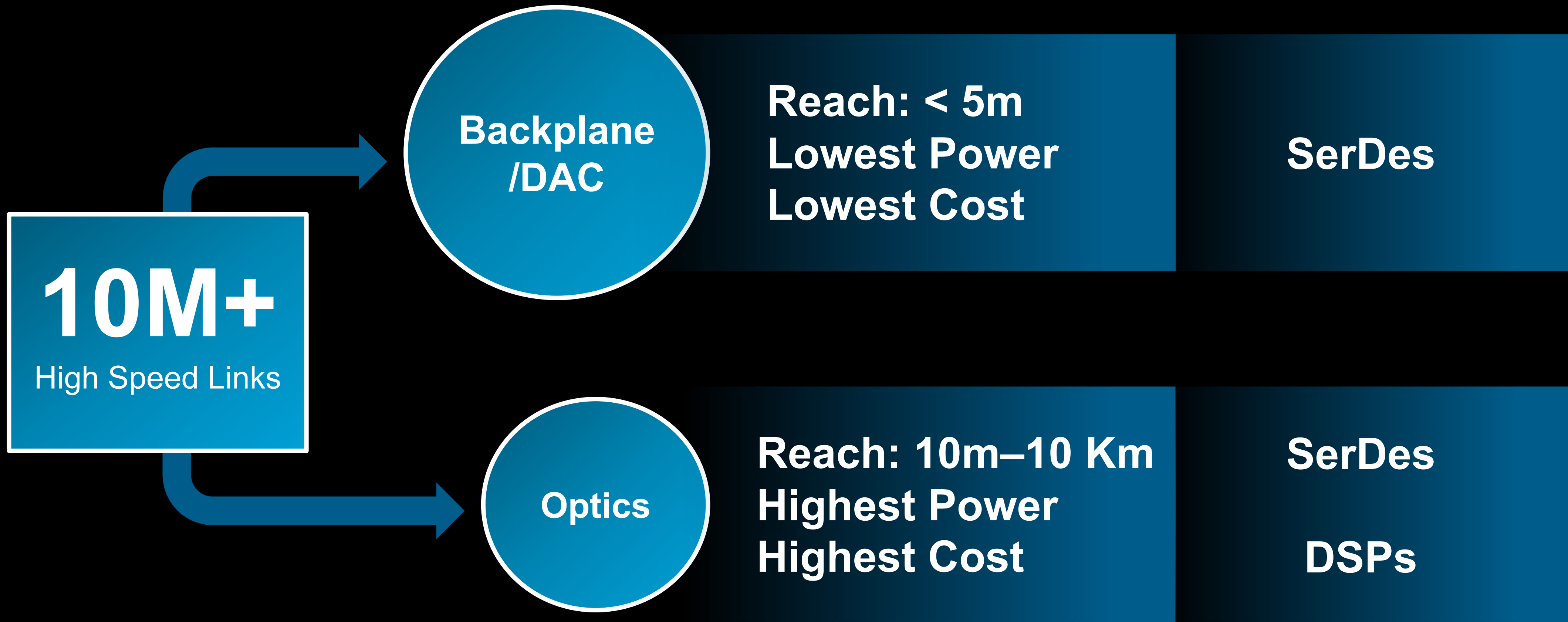
General Manager
Physical Layer Products
Broadcom





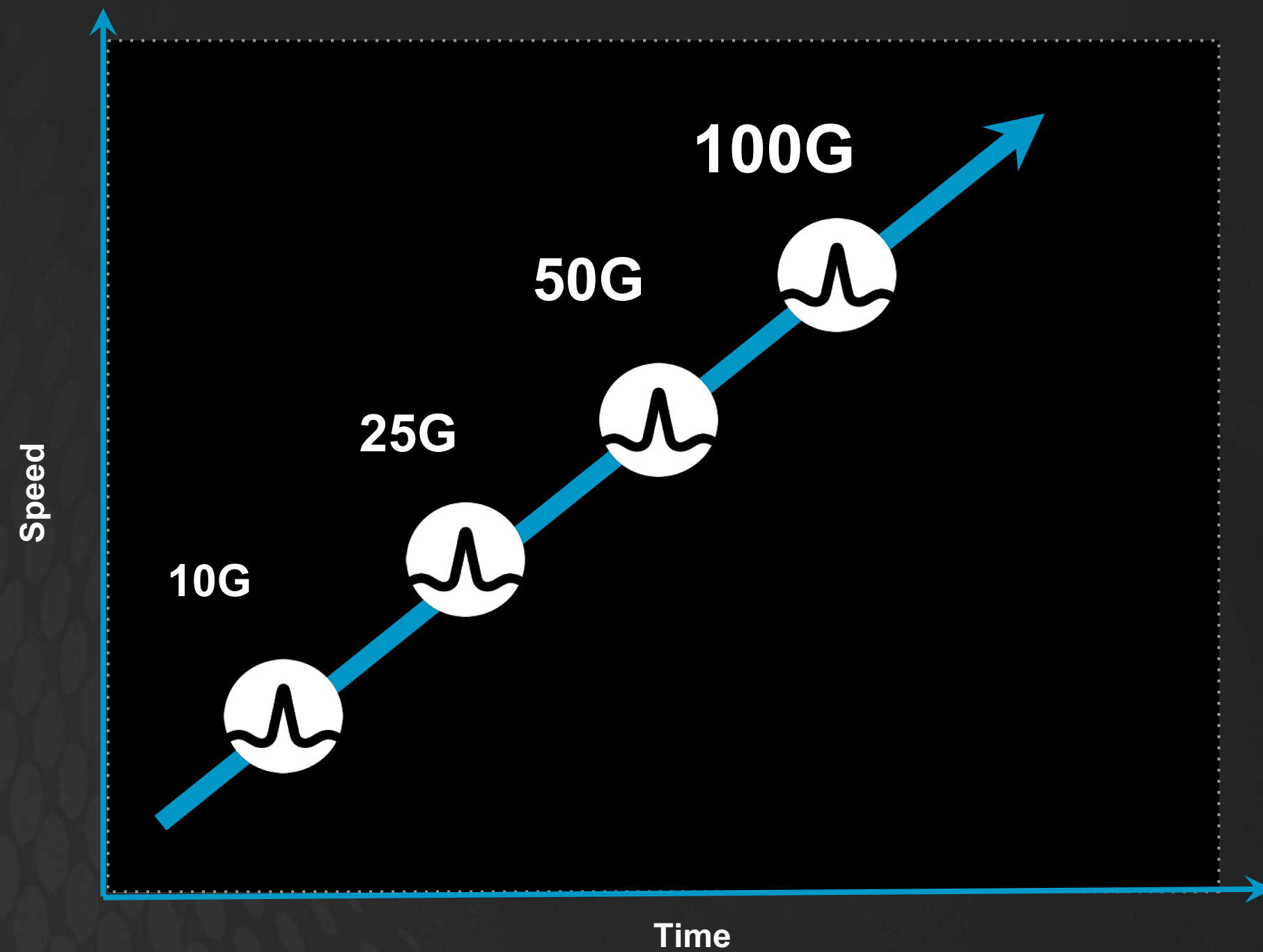
High Speed Links : 2nd Highest Power & Cost in AI Cluster

OPEN // SCALABLE // POWER EFFICIENT



Source: Broadcom Internal Estimates

OPEN // SCALABLE // POWER EFFICIENT



- High-Speed **Analog-to-Digital Conversions**
- High-Speed Custom **Digital-Signal Processing**
- Leading-Edge **Process Technology Nodes**
- **Deployment** in 100s of Systems

#1 SerDes for 4+ Generations

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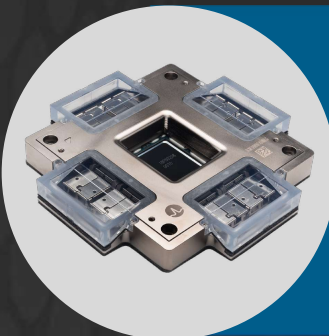
Industry-Leading 5 nm 112 Gb/s SerDes: Peregrine



45+ dB Backplanes
Higher Fanout



4+m DAC Cables
Lowest Power and Cost for Intra-Rack & Inter-Rack



Drives CPO Natively
50+% Power Reduction

New



Drives LDO Natively
33+% Power Reduction

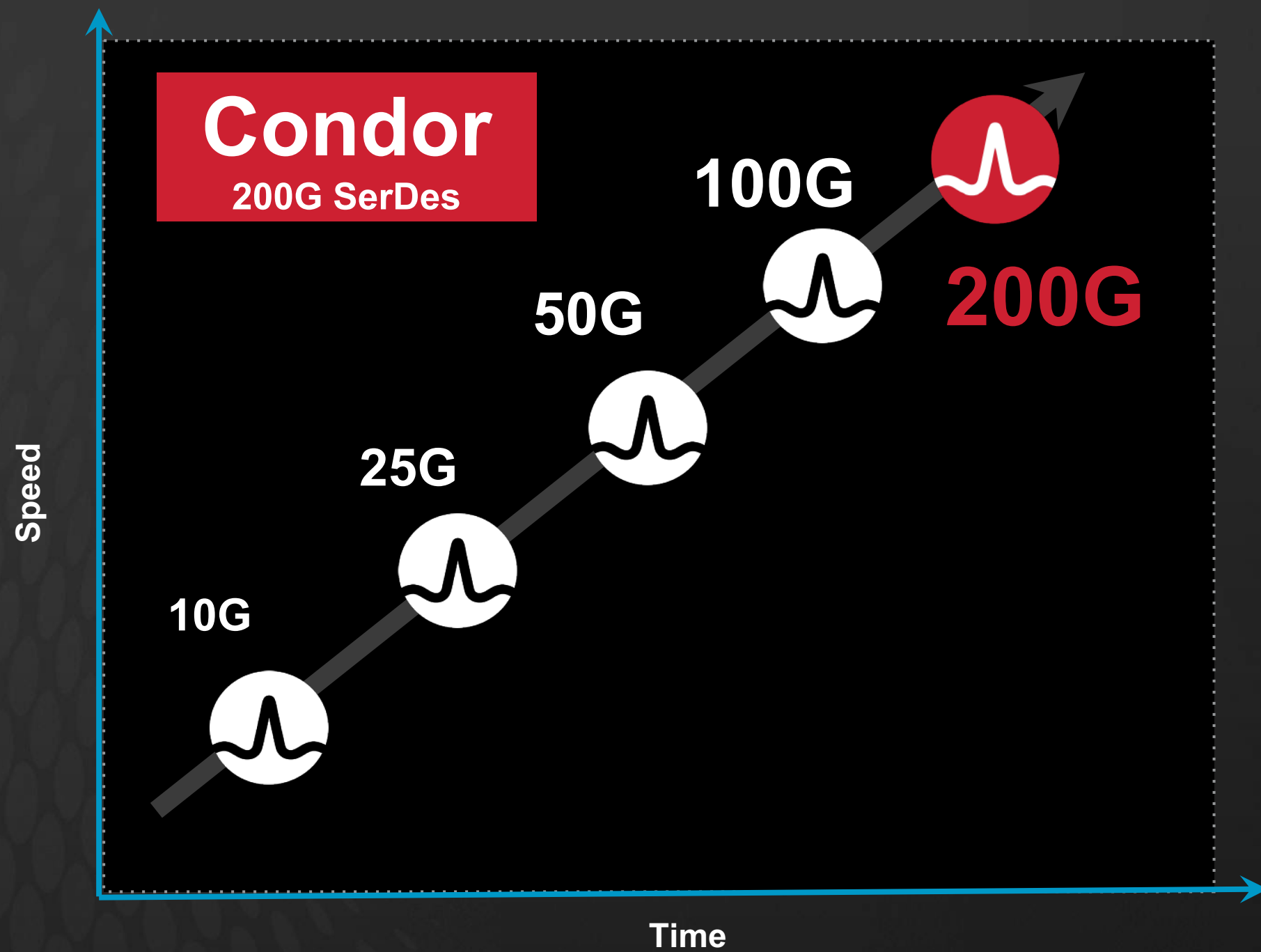
New



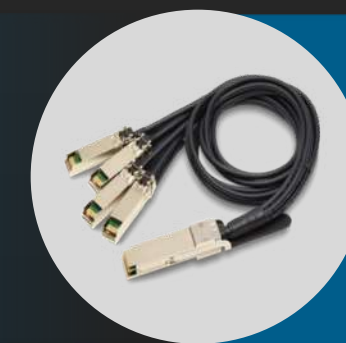
Same SerDes Benefits
Across All Broadcom Products



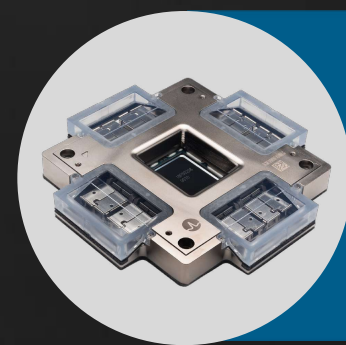
OPEN // SCALABLE // POWER EFFICIENT



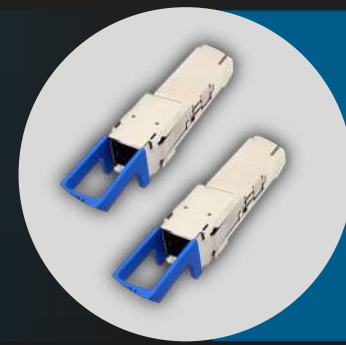
45+ dB Backplanes



2+m DAC Cables



Drives CPO



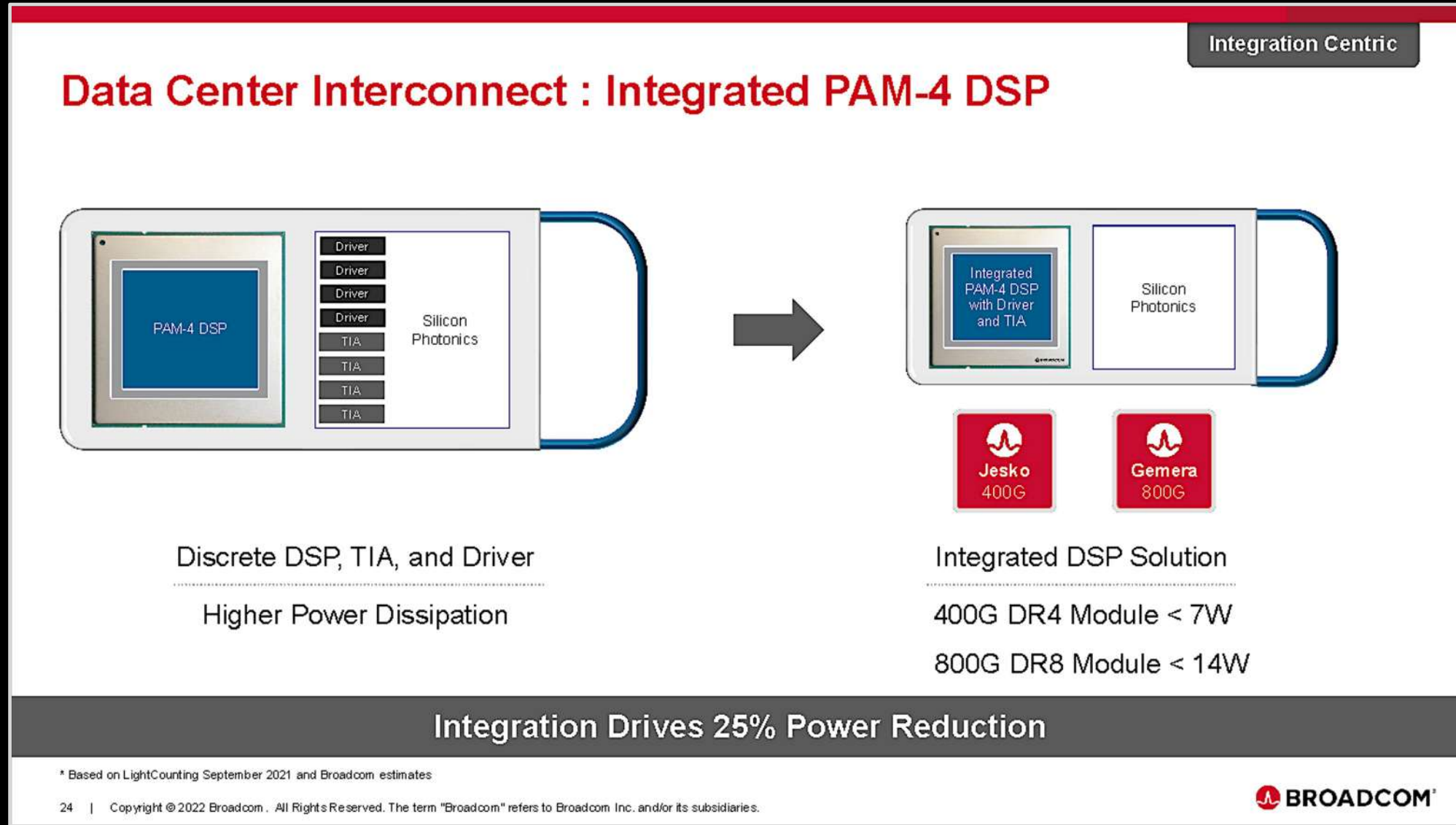
Drives LDO

Available Now

Industry's Best 200 Gb/s SerDes in 3 nm

OPEN // SCALABLE // POWER EFFICIENT

Industry's First: CMOS DSP + Driver + TIA for 100 G/λ PAM4 Optics



Promise from 4-19-2022 Teach-in: CMOS DSP + Driver + TIA

7 nm	 Jesko	400G DR4 Modules • < 7W Power
7 nm	 Gemera	800G DR8/SR8 Modules • < 14W Power
5 nm	 Cygnus	800G DR8/SR8 Modules • < 11W Power

In High-Volume Production

Broadcom iDSPs ⇒ Lowest Power/Cost MM/SM Pluggable Modules

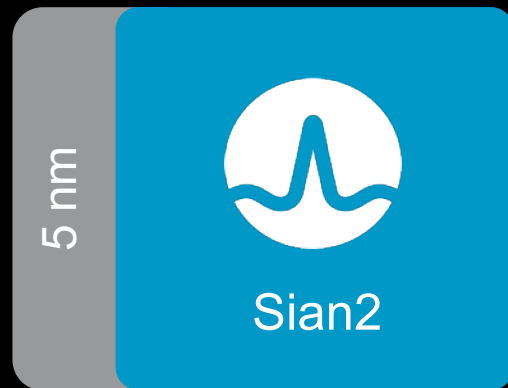
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Best-Performing 200 G/λ DSPs in the Industry



1.6T DR8 Modules

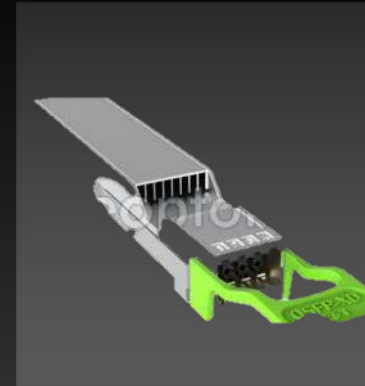
- 16x100G to 8x200G
- 212 Gb/s FEC Bypass
- 226 Gb/s w/ Inner FEC
- Integrated Driver



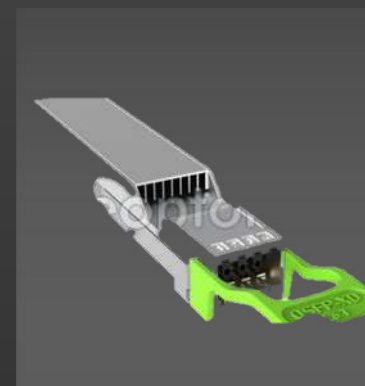
1.6T DR8 Modules

- 8x200G to 8x200G
- 212 Gb/s FEC Bypass
- 226 Gb/s w/ Inner FEC
- Integrated Driver

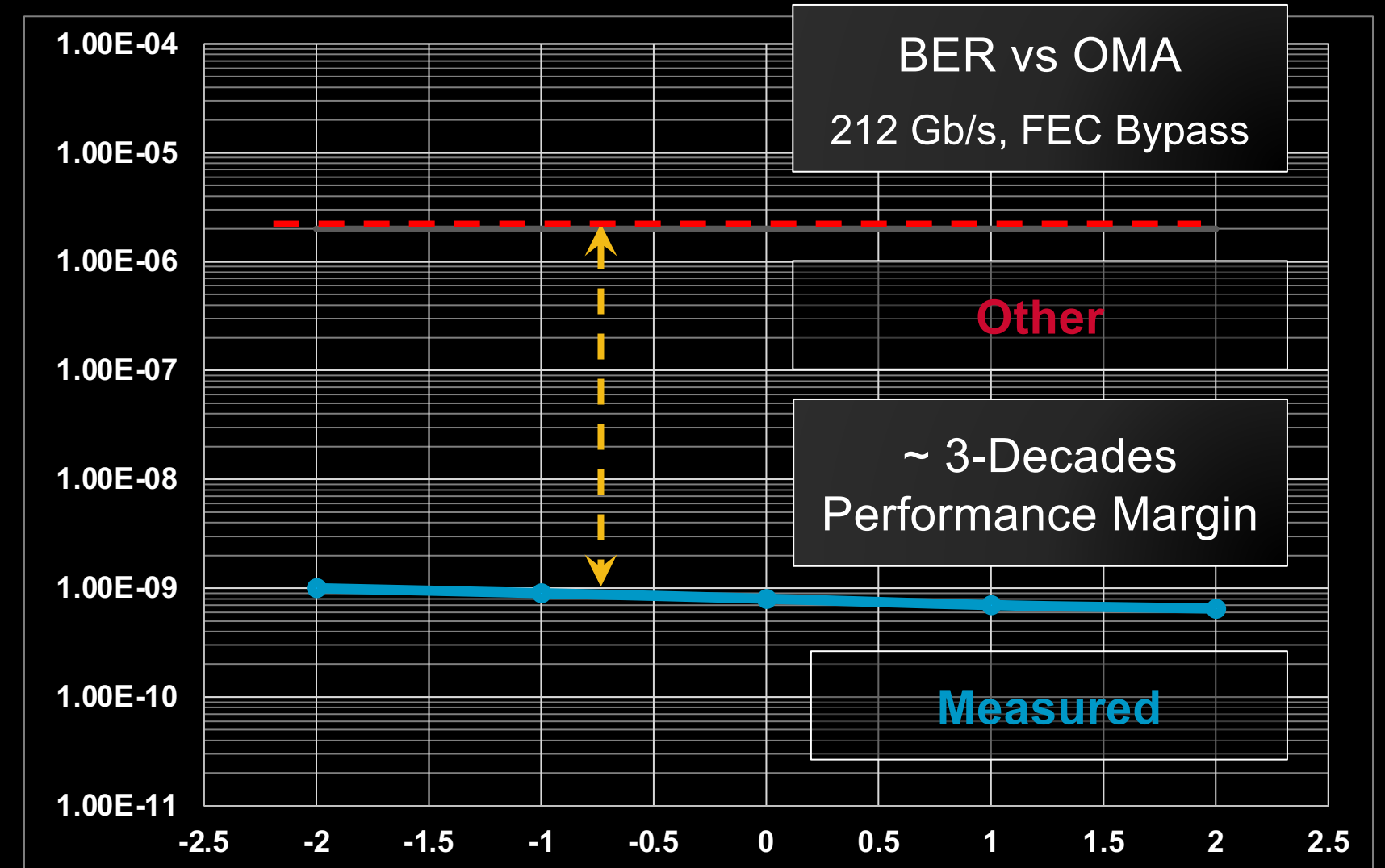
Integrated DSPs for 1.6T Generation



MMF



SMF



Performance Result from Partner 1.6T Module

200G iDSPs ⇒ Performance, Power and Latency Leadership

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Foundation Technology



100 Gb/s **BEST-IN-CLASS** Innovative Connectivity

Key Points



200 Gb/s **LEADS** Open Ecosystem



DIFFERENTIATION from Analog + DSP Expertise, R&D Scale

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ENABLING AI Infrastructure

Custom Accelerators
(XPU's)

Frank Ostojic

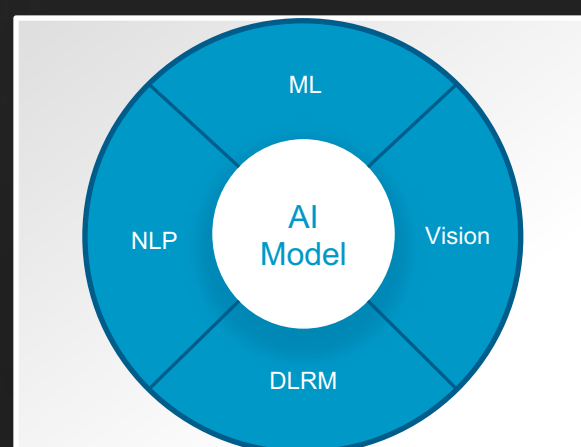
General Manager
Custom AI Product Division
Broadcom



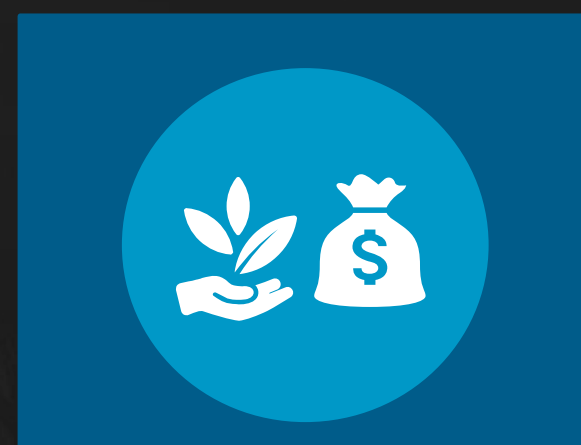
#1 in **custom silicon**
for **10 years**

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Consumer AI Requires Custom Accelerators (XPU)



Architecture optimized for internal workloads



Larger volumes → lower power & cost



Memory & I/O architecture customized for AI workloads

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Industry-Leading IP Portfolio for Differentiated XPU's

SerDes IP

AI-Optimized NICs IP

Advanced Pkg

Jericho3-AI

Switching IP Cores

Co-Packaged Optics

Buffer Memory IP

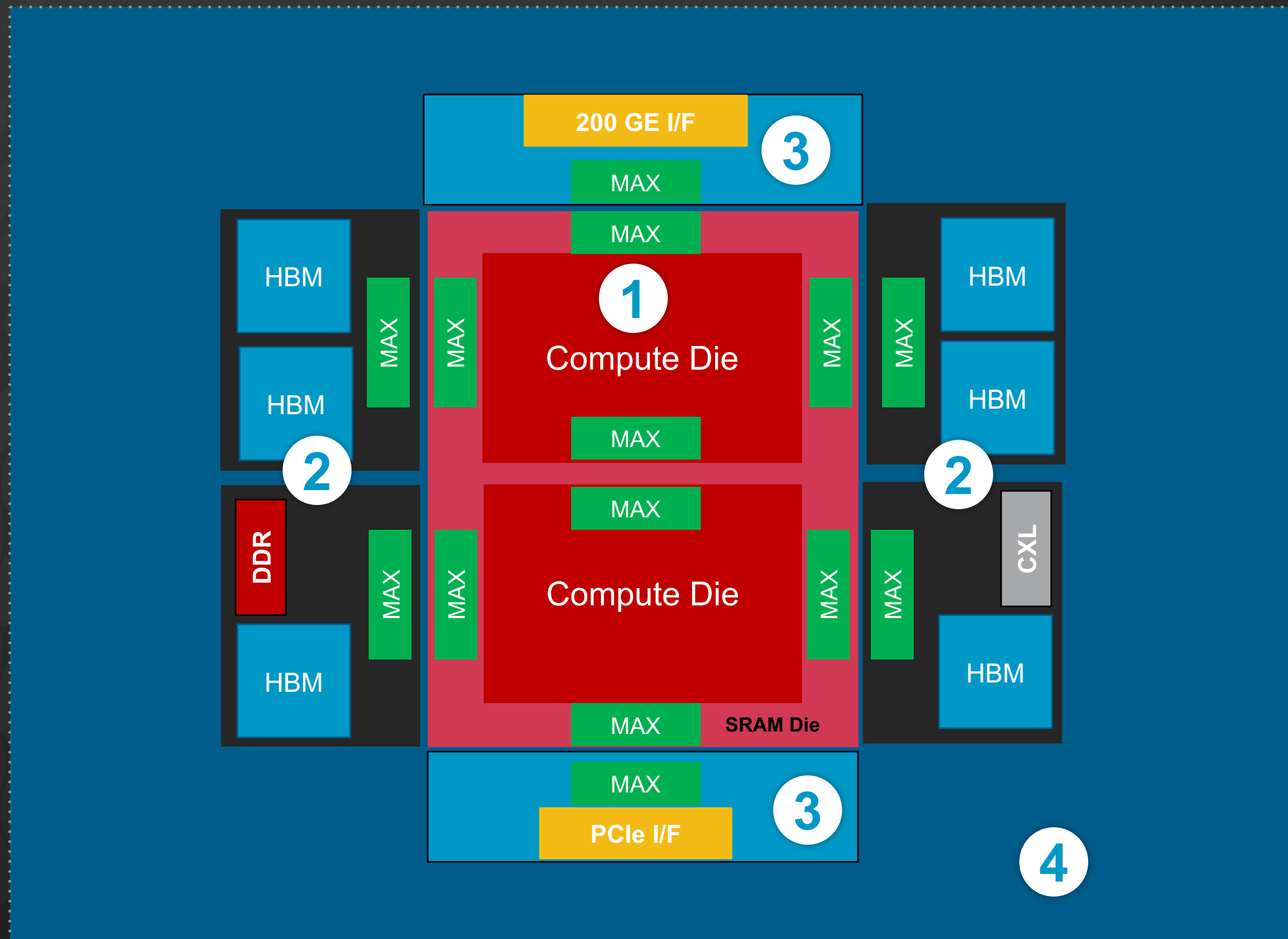
\$3B+
R&D Investment



Optimized Architecture + Lowest Power → Best Performance/TCO

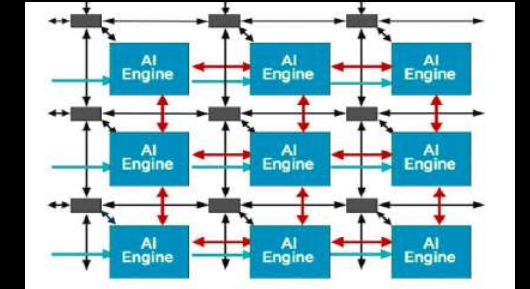
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Broadcom IP Enables XPU Critical Components



1 Compute

Processing Unit Architecture (Customer Owned)
Design Flow & Performance Optimization (Broadcom Owned)



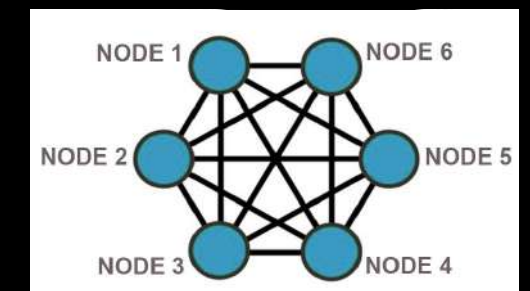
2 Memory

HBM PHY, Integration & Performance (Broadcom Owned)



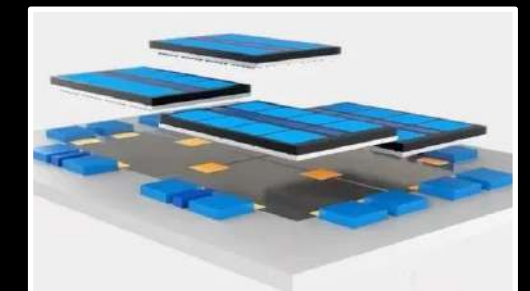
3 Network IO

Architecture & Implementation (Broadcom Owned)
Full Solution Chiplets (Hardware, Firmware, & Software)



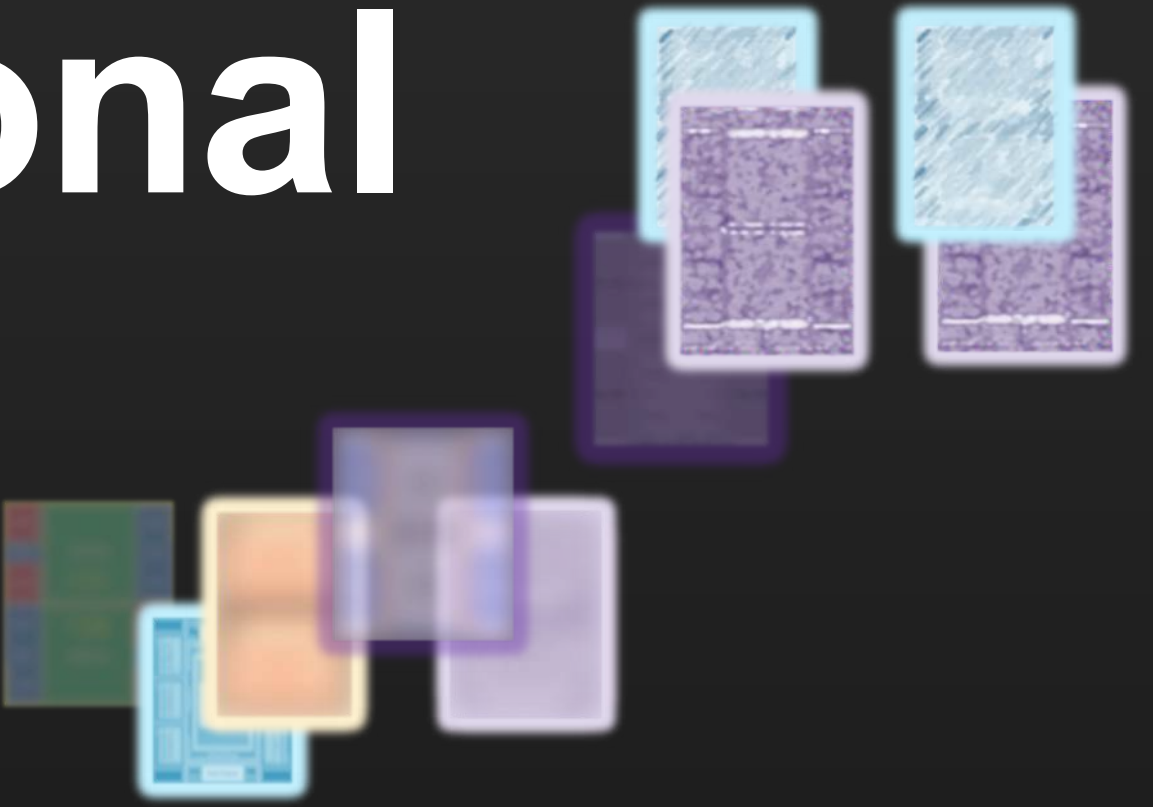
4 Package

2.5D, 3D, & Silicon Photonics Architecture & Implementation (Broadcom Owned); Vertical Integration Advantage



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Delivering Multi-Generational Custom AI Accelerators over the Past Decade



2014

2021

2022-2023

2024-2025

2026 & Beyond

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Deep, Strategic, Multi-Year Partnership with Consumer AI Customers



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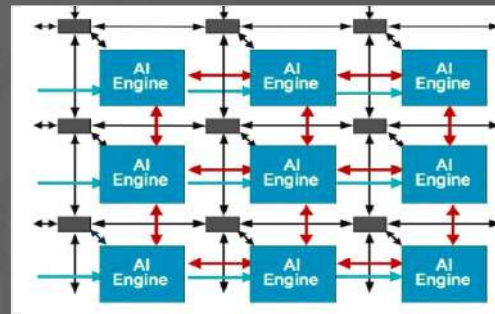
Industry's Fastest Time-to-Production with Annual Cadence

XPU Platform Engineering
Years prior to Design Start

7–9 Month
Development

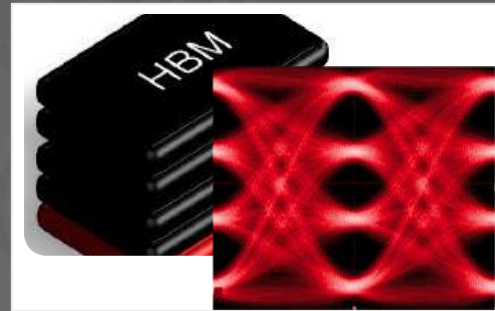
FAB

3-Month
Production
Ramp



**Automated
Design
Flow**

AI Design Flow Optimized over
10 Years of XPU experience



AI IP

Plug & Play Ready

- ✓ Silicon
- ✓ Firmware
- ✓ Software-API



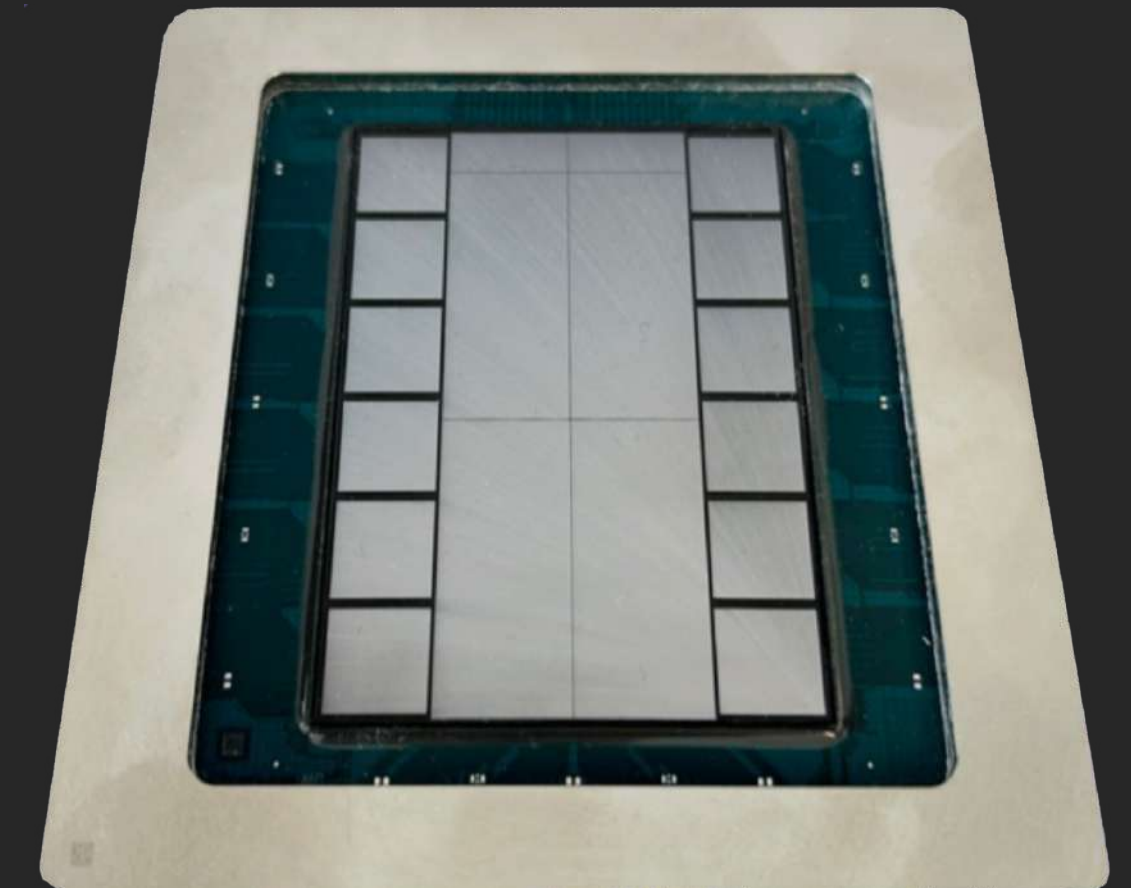
**SOC
Package**

Pre-Qualified

- ✓ Thermal
- ✓ Mechanical
- ✓ Electrical



**Co-Development
with
Consumer
AI Customer**



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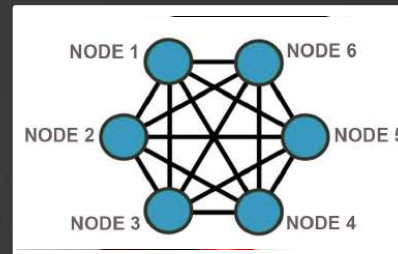
Deep & Strategic Collaboration During Architectural Phase

INVESTMENT PERIOD
2023-2025

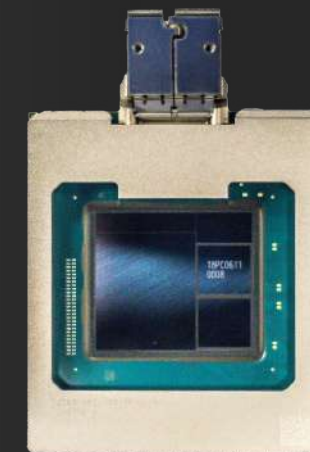
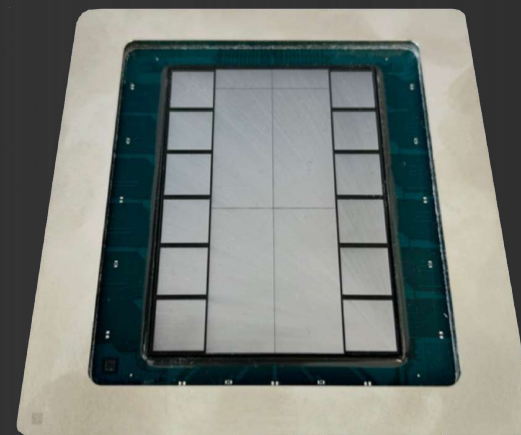
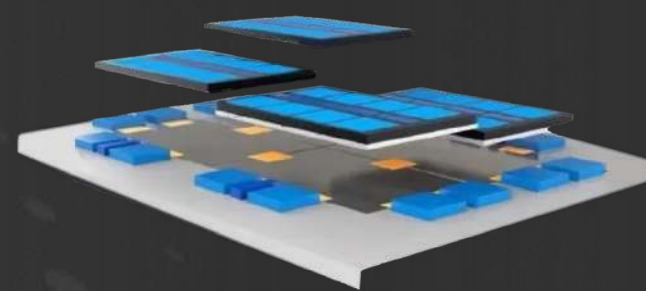
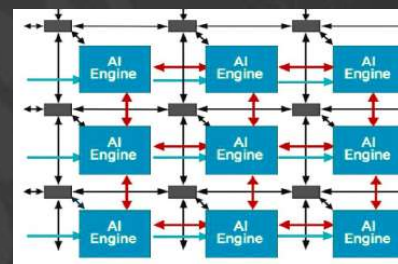
ARCHITECTURE PHASE
2026 & Beyond



Early IP investments years before XPU design kick-off across critical components

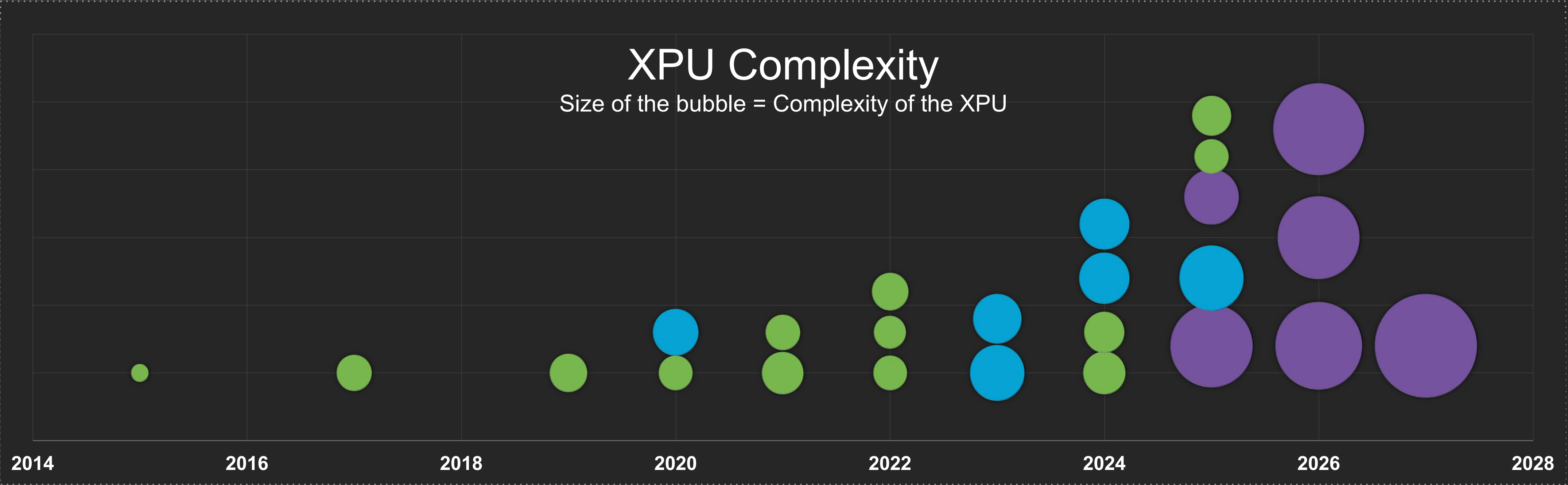








Concurrent technology, IP & packaging investments for next two generations of XPUs



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Execution Excellence in Delivering to Consumer-AI Requirements



$F(\text{Complexity}) = \{\text{Compute Performance, Network Bandwidth, Memory Bandwidth, Power Delivery, Thermal Integrity, Mechanical Reliability}\}$

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Custom AI Accelerators

Key Points



Focused on Consumer-AI Custom Accelerators



\$3B+ Investment Scale in Differentiation **XPU IP**



10-year Engineering Excellence in High-Complexity XPU's



3-year Deep Architectural Advantage in Co-Development

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ENABLING AI Infrastructure

Charlie Kawwas, Ph. D.
President, Broadcom



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Consumer AI

Search, Social Networking, ...

Enterprise AI

Public Cloud, On-Prem, ...

AI Accelerators (XPU)

Custom

Merchant

AI Connectivity

Merchant

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XPUs → Multi-Generational Strategic Engagements

2024

2025

2026

Customer #1

Production



Customer #2

Production



Customer #3

New

Ramp →
Production



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Broadest & Industry-Leading AI Networking Portfolio

Ethernet

Broadcom (AVGO) to Deploy World's First 51.2 Tbps Switches
source: Yahoo Finance

New Chip on the Block: Broadcom's Jericho3-AI can Connect Up to 32000 GPU Chips
source: Interesting Engineering

Broadcom Qumran3D 5nm 25.6T Switch Router Chip
source: ServeTheHome

Broadcom Adds AI Features to Speed New Trident Networking Chip
source: Reuters

PCIe

Industry's First End-to-End PCIe/CXL Connectivity Portfolio

PCIe/CXL Switches

PCIe/CXL Retimers

BROADCOM

Optics

Broadcom Upgrades Co-Packaged Optics Switch to 51.2Tb/s
source: Electronic Design

World Leader in AI Infrastructure Optics

EML

VCSEL

CW Laser

BROADCOM

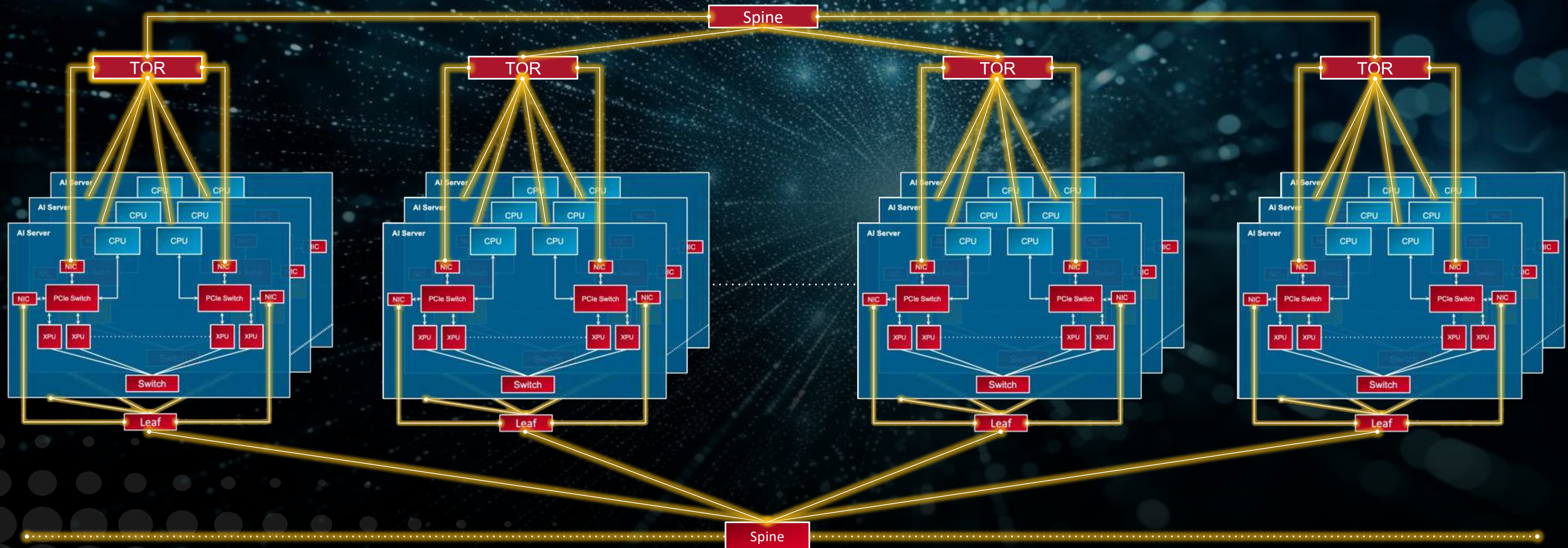
Foundational Technology

Broadcom Delivers 200G/lane PAM-4 DSP PHY for Next-Gen Switches and AI Networks
Source: Yahoo Finance

Broadcom Introduces Industry's First 5nm 100G/lane Optical
source: GlobeNewswire

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... Enabling AI Infrastructure



OPEN // SCALABLE // POWER EFFICIENT

Open Scalable Power Efficient

Sustainable Technology Leadership

Ethernet PCIe Optics SerDes DSP Custom

Investment Scale

Innovation Leadership

Execution Excellence

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Thank you

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ENABLING AI Infrastructure

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